Lecture 04

CHAPTER 3 - CMOS MODELS

Chapter Outline

3.1 MOS Structure and Operation
3.2 Large signal MOS models suitable for hand calculations
3.3 Extensions of the large signal MOS model
3.4 Capacitances of the MOSFET
3.5 Small Signal MOS models
3.6 Temperature and noise models for MOS transistors
3.7 BJT models
3.8 SPICE level 2 model
3.9 Models for simulation of MOS circuits
3.10 Extraction of a large signal model for hand calculations from the BSIM3 model
3.11 Summary

Perspective

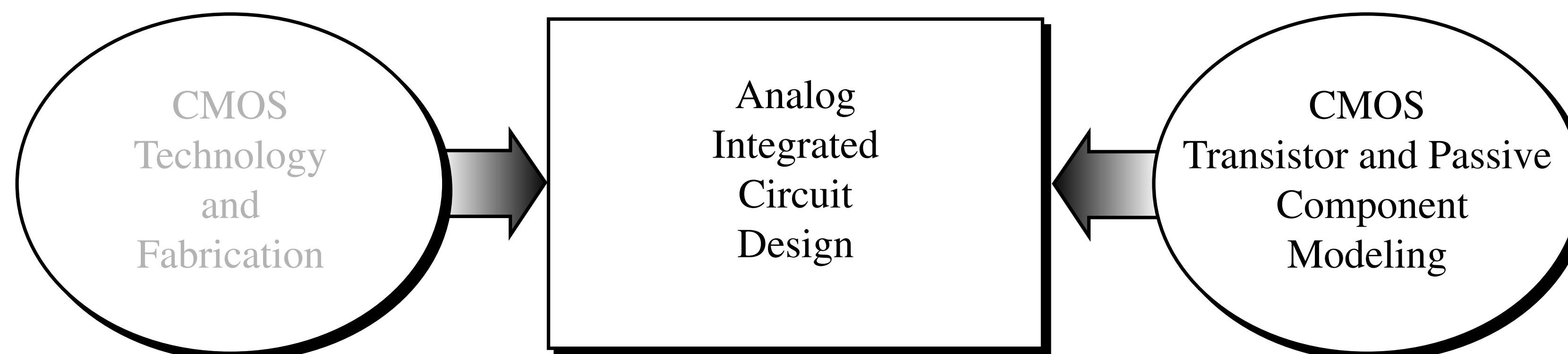

Fig.3.0-1

Philosophy for Models Suitable for Analog Design

The model required for analog design with CMOS technology is one that leads to understanding and insight as distinguished from accuracy.

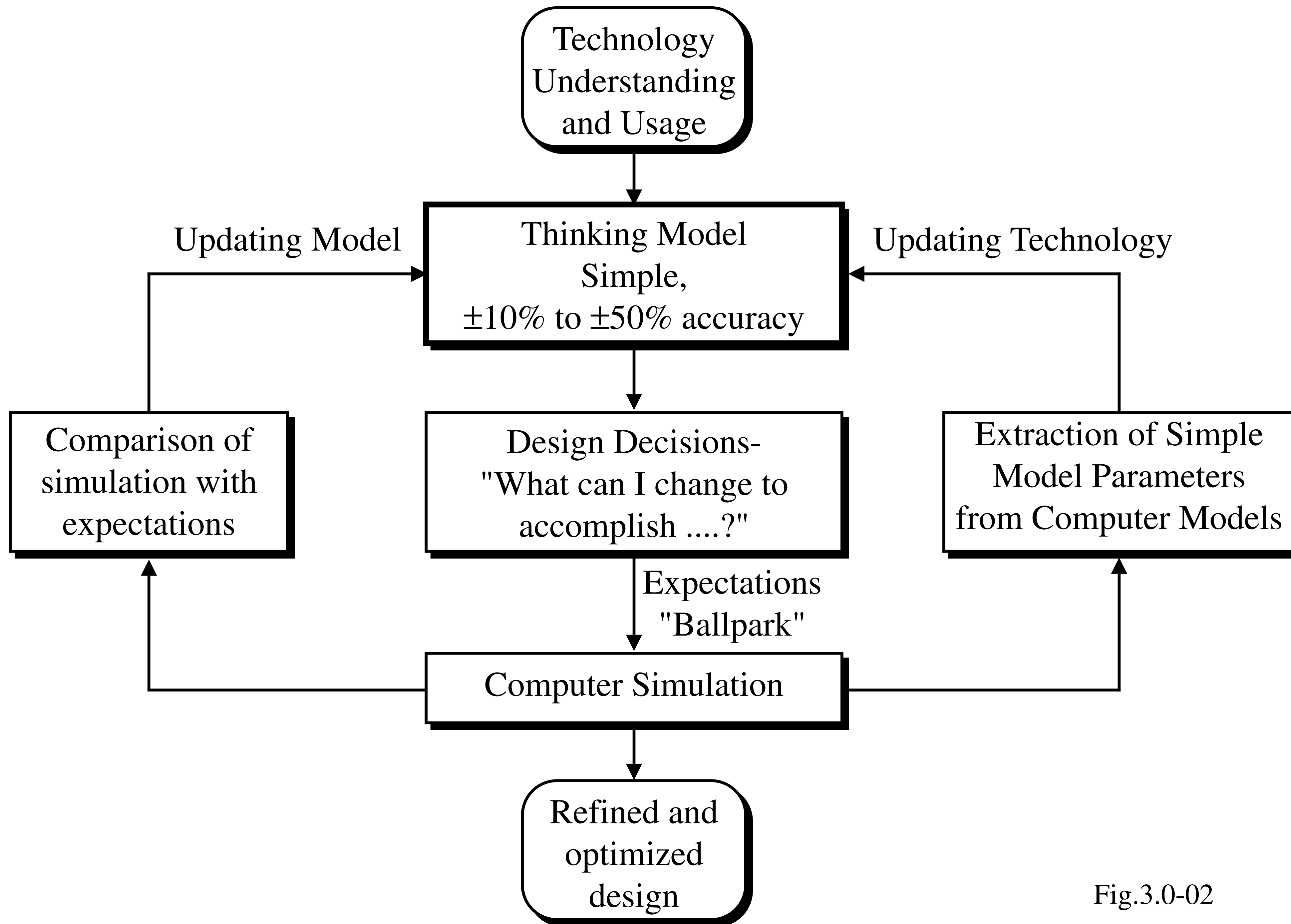

Fig.3.0-02

This chapter is devoted to the simple model suitable for design *not* using simulation.

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Categorization of Electrical Models

		Time Dependence	
		Time Independent	Time Dependent
Linearity	Linear	Small-signal, midband R_{in}, A_v, R_{out} (.TF)	Small-signal frequency response-poles and zeros (.AC)
	Nonlinear	DC operating point $i_D = f(v_D, v_G, v_S, v_B)$ (.OP)	Large-signal transient response - Slew rate (.TRAN)

Based on the simulation capabilities of SPICE.

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3.1 - MOS STRUCTURE AND OPERATION

Metal-Oxide-Semiconductor Structure

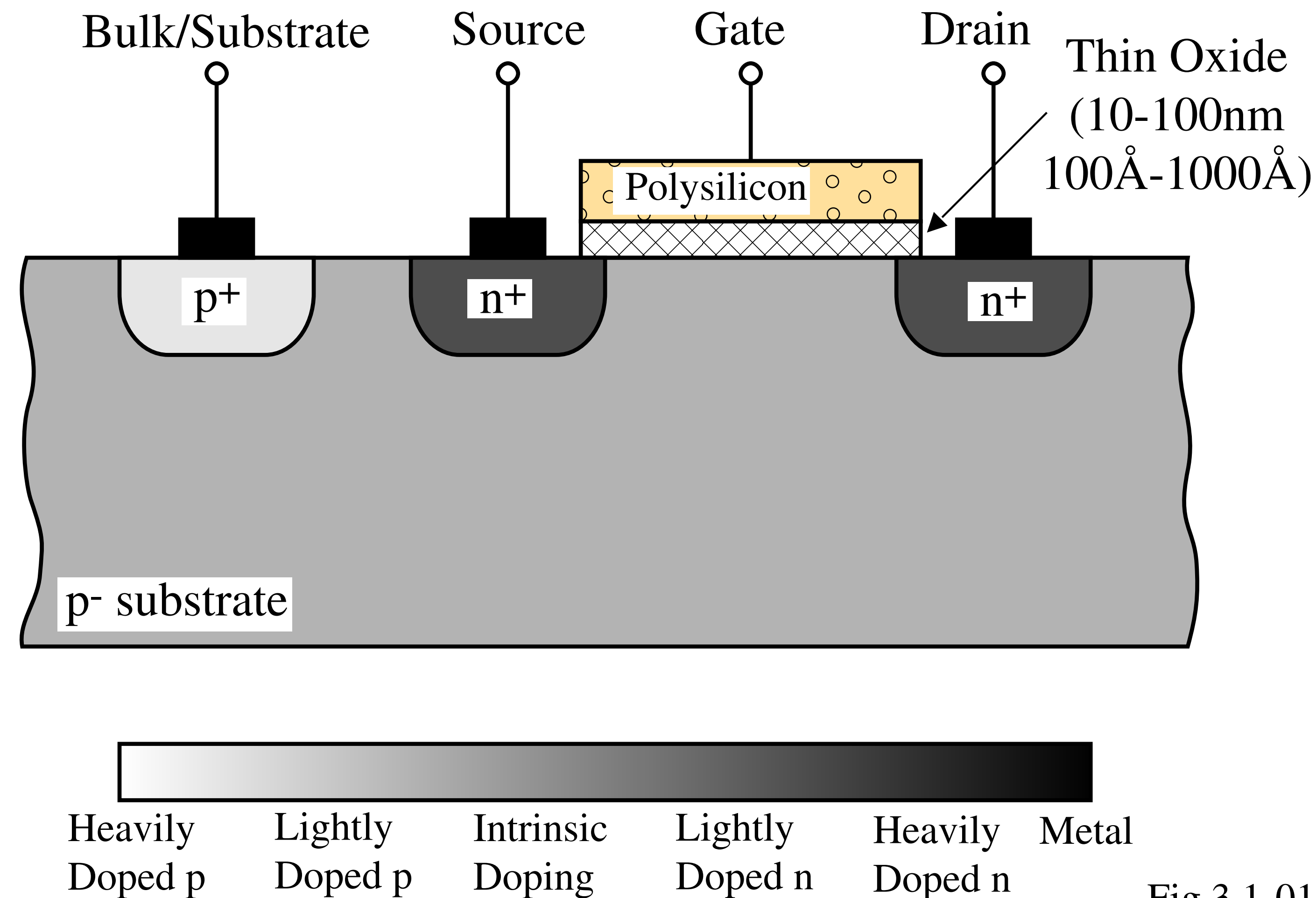

Fig.3.1-01

Terminals:

- Bulk - Used to make an ohmic contact to the substrate
- Gate - The gate voltage is applied in such a manner as to invert the doping of the material directly beneath the gate to form a channel between the source and drain.
- Source - Source of the carriers flowing in the channel
- Drain - Collects the carriers flowing in the channel

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Formation of the Channel for an Enhancement MOS Transistor

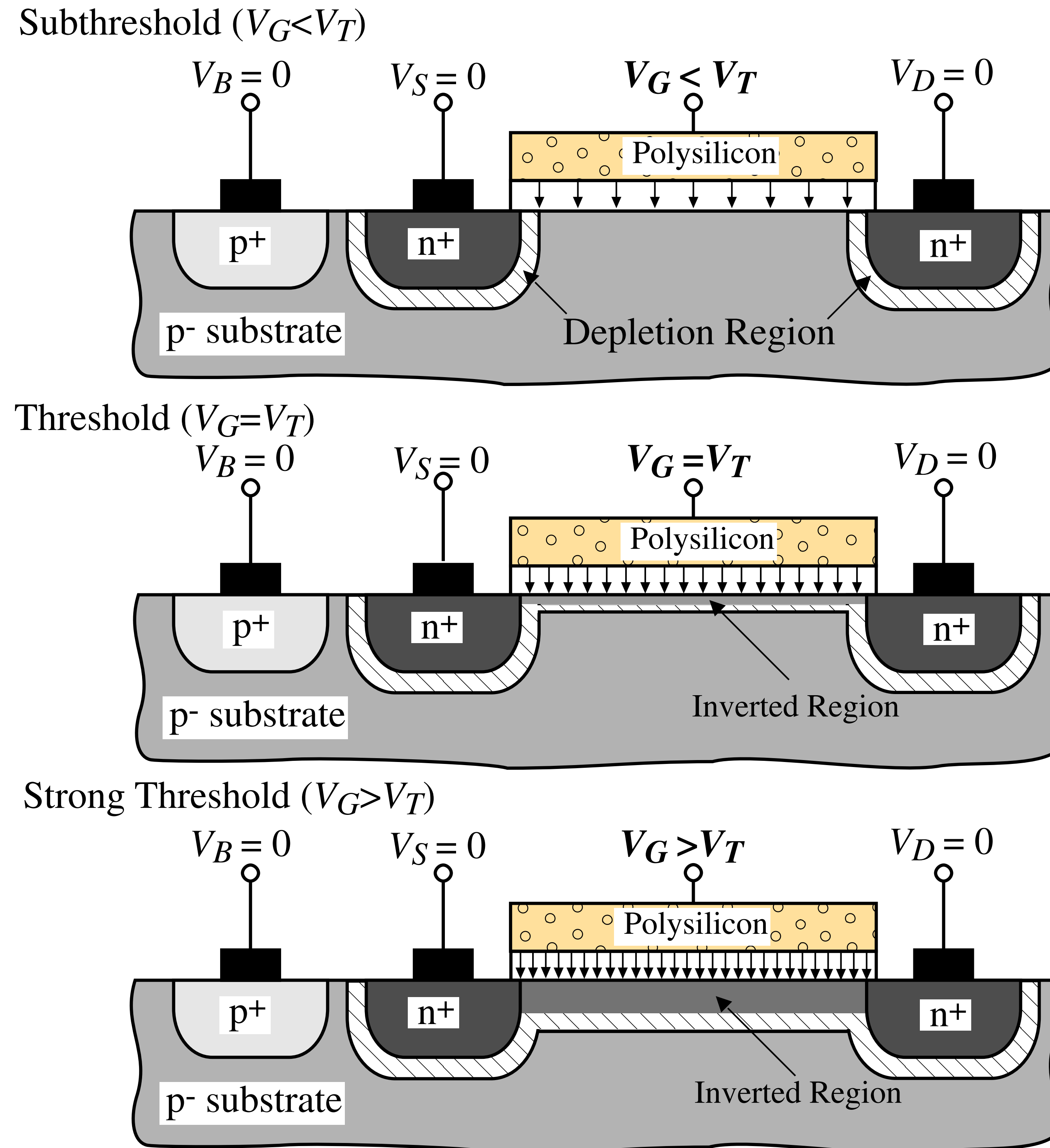

Fig.3.1-02

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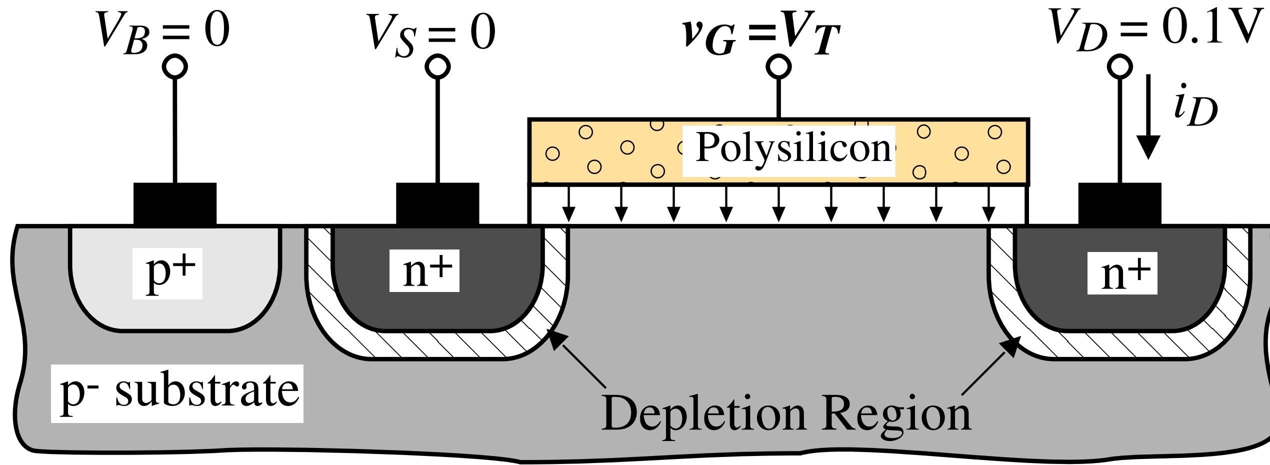
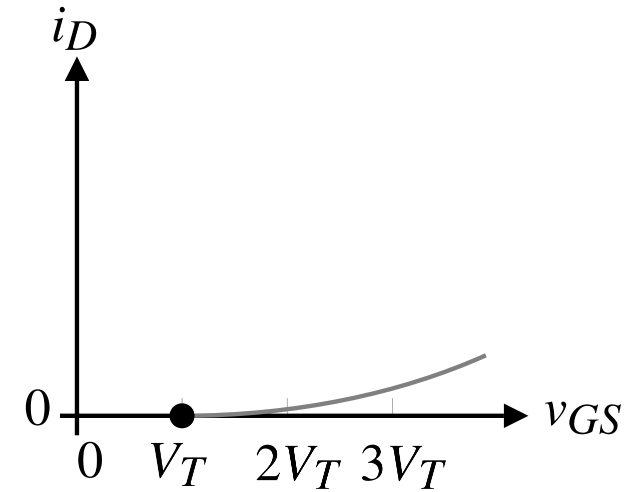
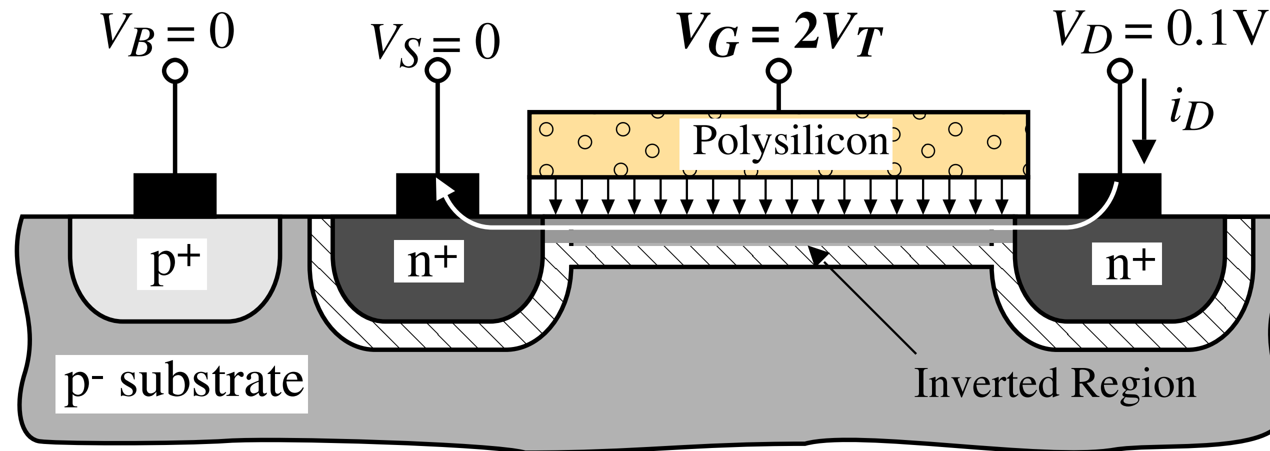
Transconductance Characteristics of an Enhancement NMOS FET when $V_{DS} = 0.1\text{V}$

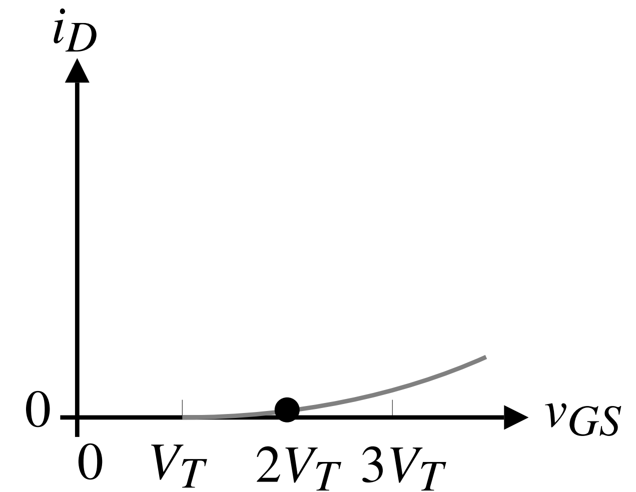
$V_{GS} \le V_T$:



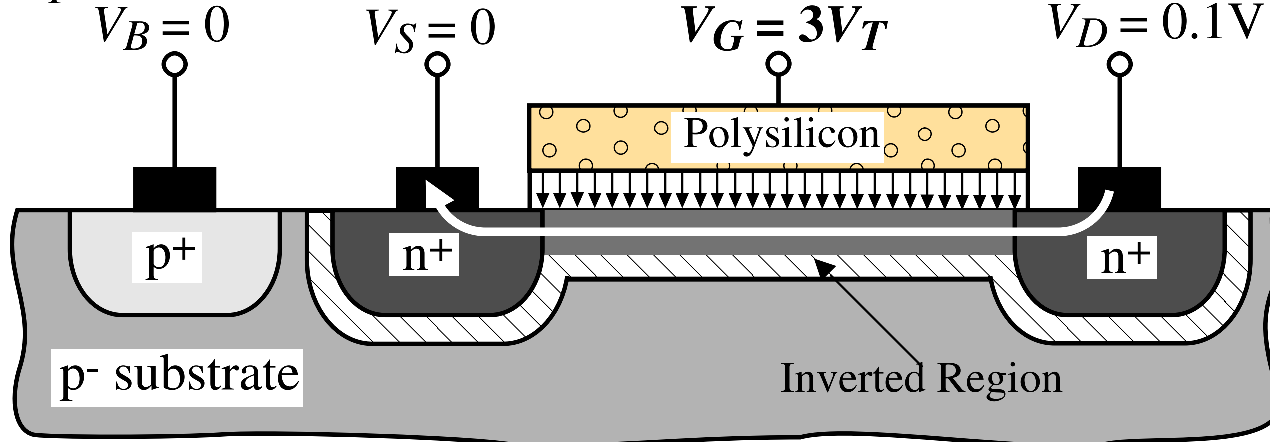


$V_{GS} = 2V_T$:





$V_{GS} = 3V_T$:



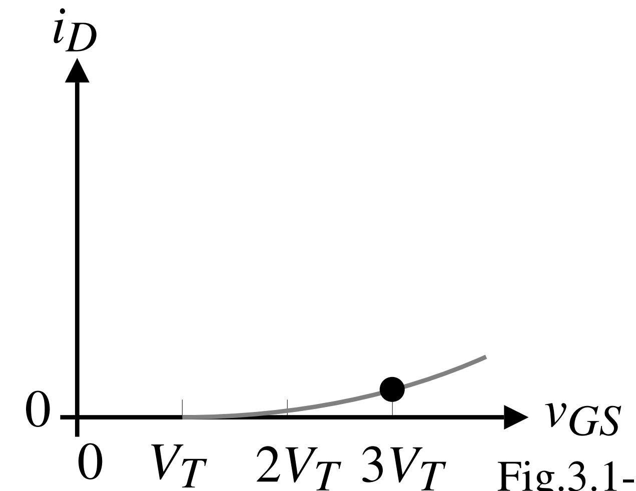


Fig.3.1-03

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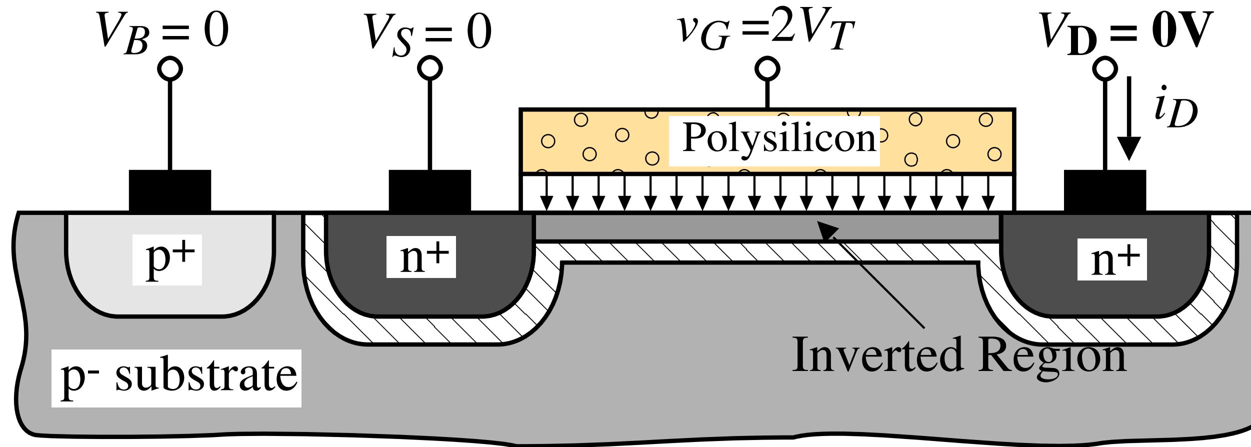
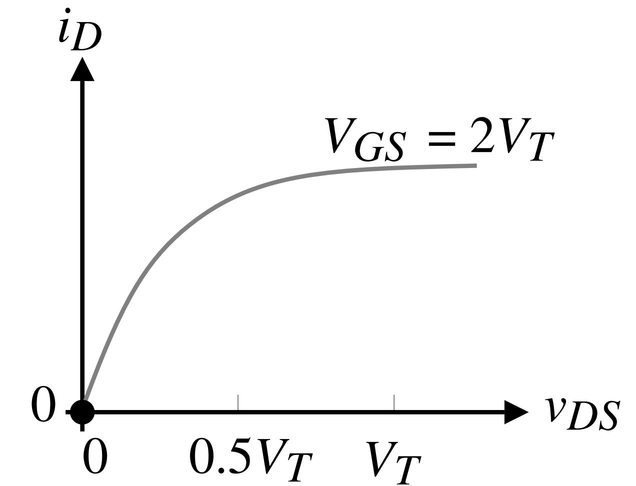
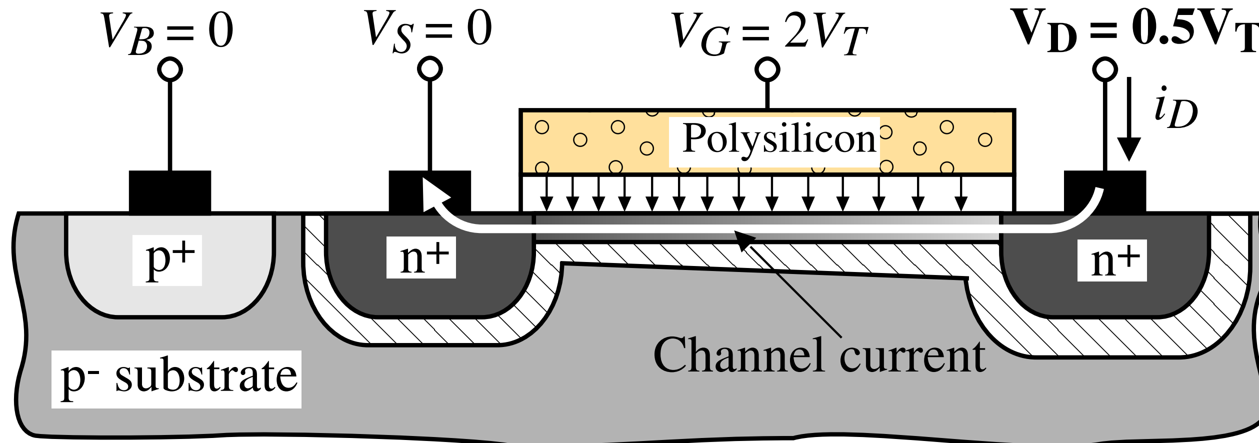
Output Characteristics of the Enhancement NMOS Transistor for $V_{GS} = 2V_T$

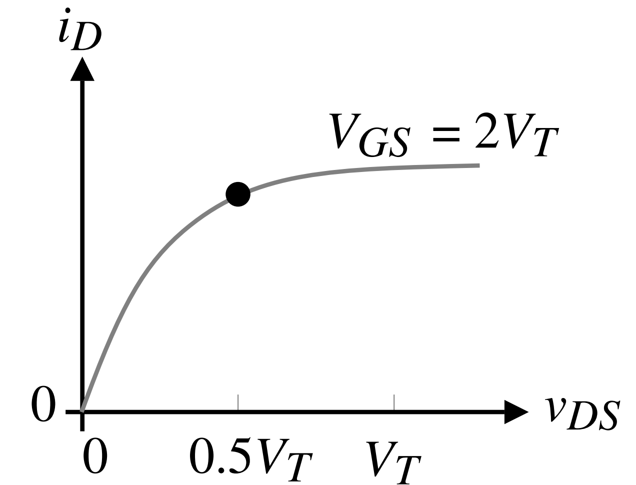
V_{DS}=0:



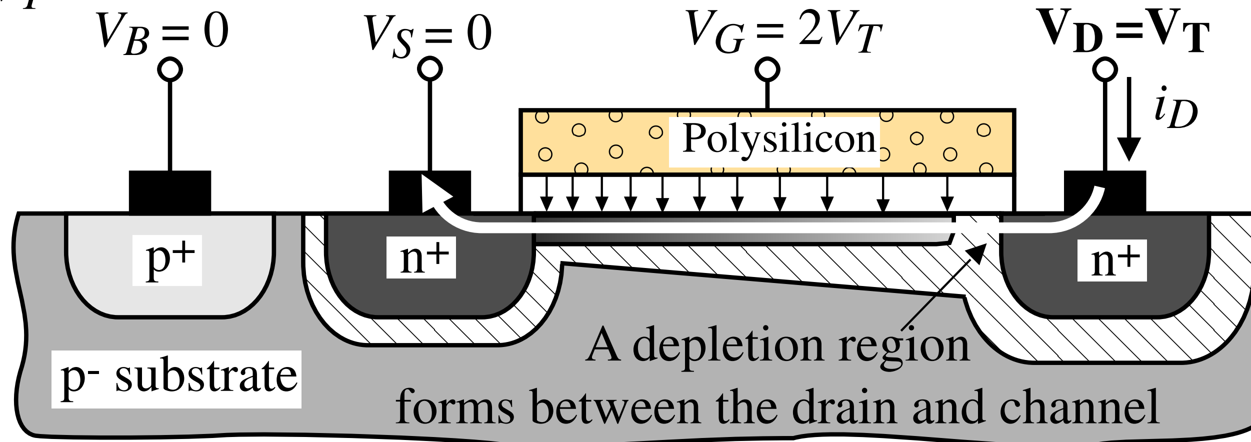


V_{DS}=0.5V_T:





V_{DS}=V_T:



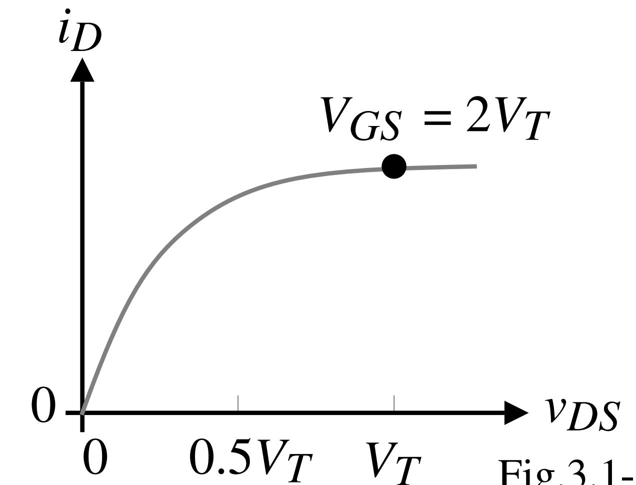


Fig.3.1-04

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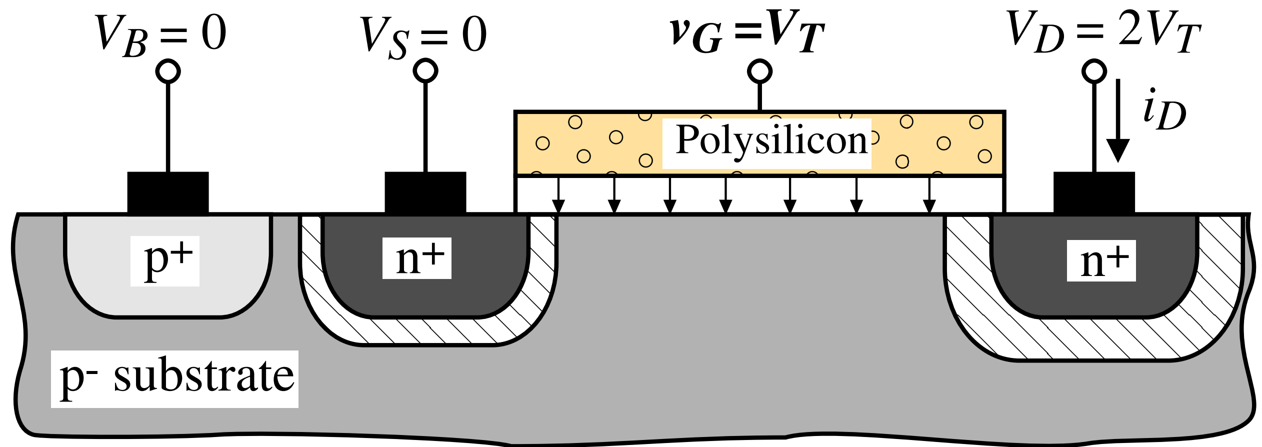
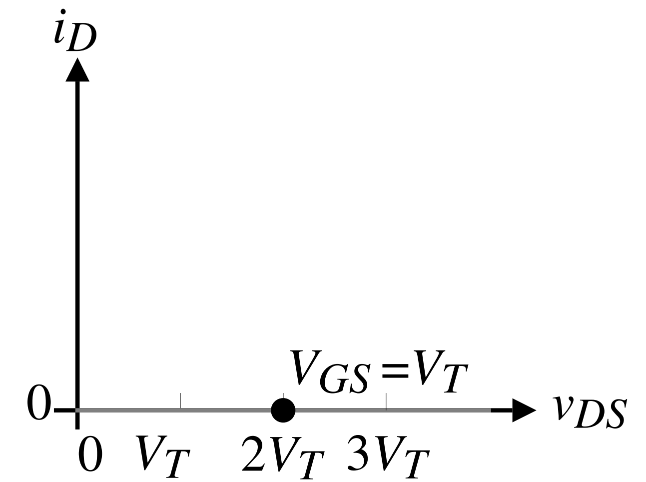
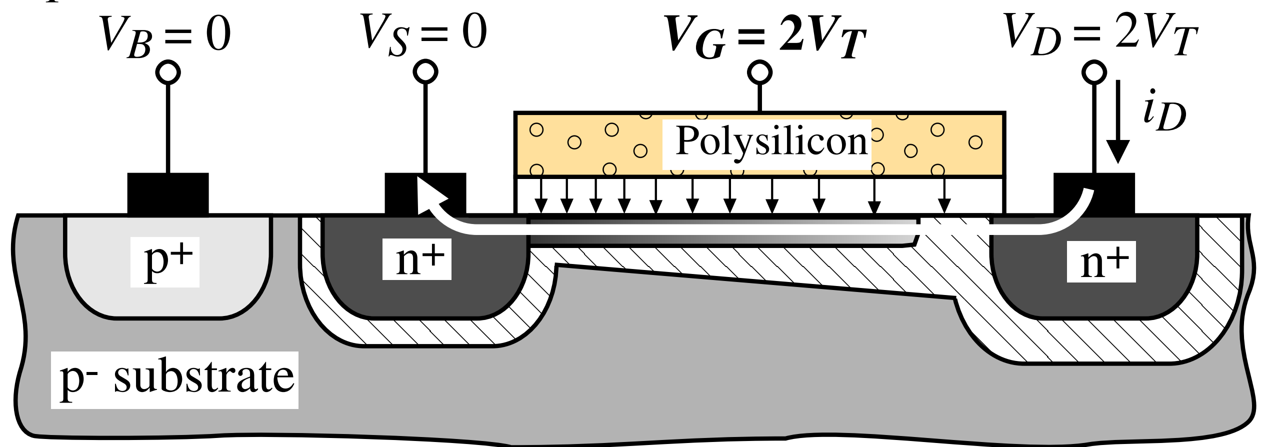
Output Characteristics of the Enhanced NMOS when $v_{DS} = 2V_T$

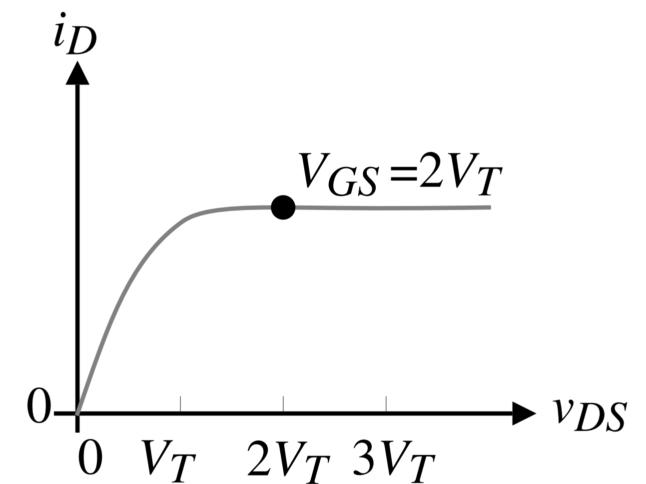
$V_{GS}=V_T$:



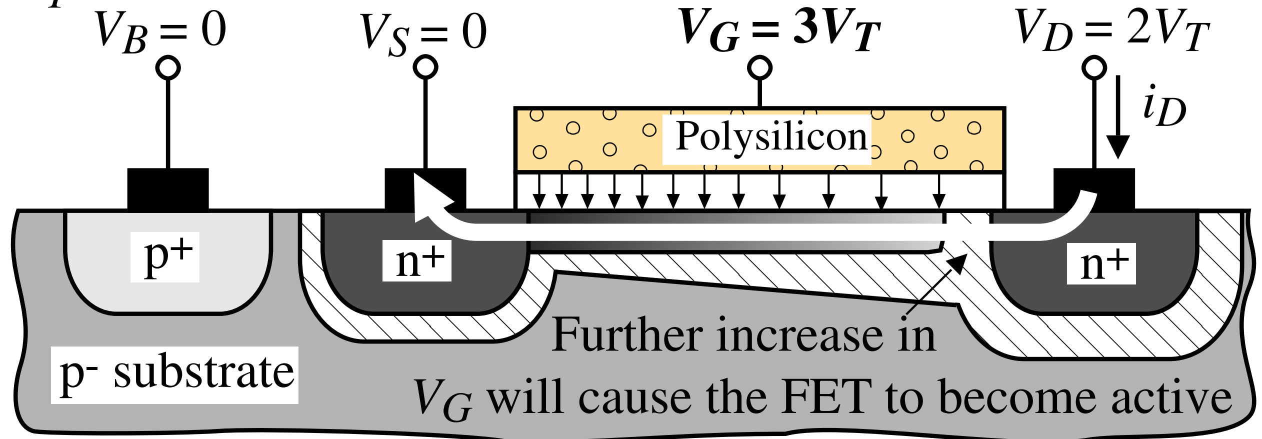


$V_{GS}=2V_T$:





$V_{GS}=3V_T$:



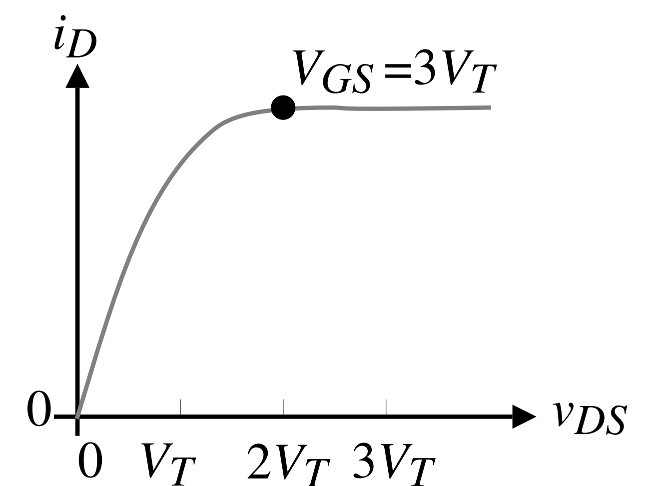


Fig.3.1-05

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Output Characteristics of an Enhancement NMOS Transistor

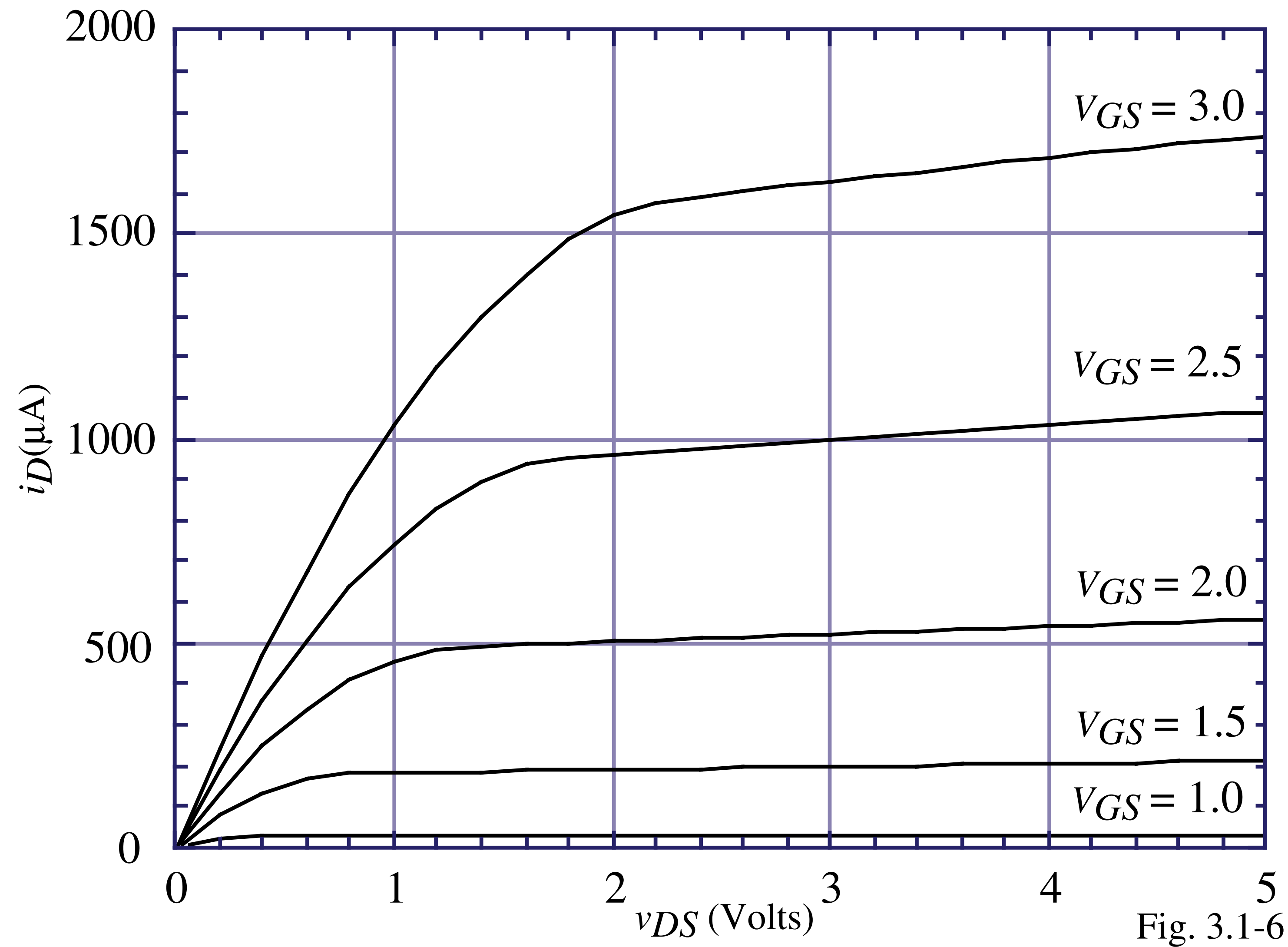

Fig. 3.1-6

SPICE Input File:

```
Output Characteristics for NMOS
M1 6 1 0 0 MOS1 w=5u l=1.0u
VGS1 1 0 1.0
M2 6 2 0 0 MOS1 w=5u l=1.0u
VGS2 2 0 1.5
M3 6 3 0 0 MOS1 w=5u l=1.0u
VGS3 3 0 2.0
M4 6 4 0 0 MOS1 w=5u l=1.0u
VGS4 4 0 2.5
M5 6 5 0 0 MOS1 w=5u l=1.0u
VGS5 5 0 3.0
VDS 6 0 5
.model mos1 nmos (vto=0.7 kp=110u
+gamma=0.4 +lambda=.04 phi=.7)
.dc vds 0 5 .2
.print dc ID(M1), ID(M2), ID(M3), ID(M4),
ID(M5)
.end
```

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Transconductance Characteristics of an Enhancement NMOS Transistor

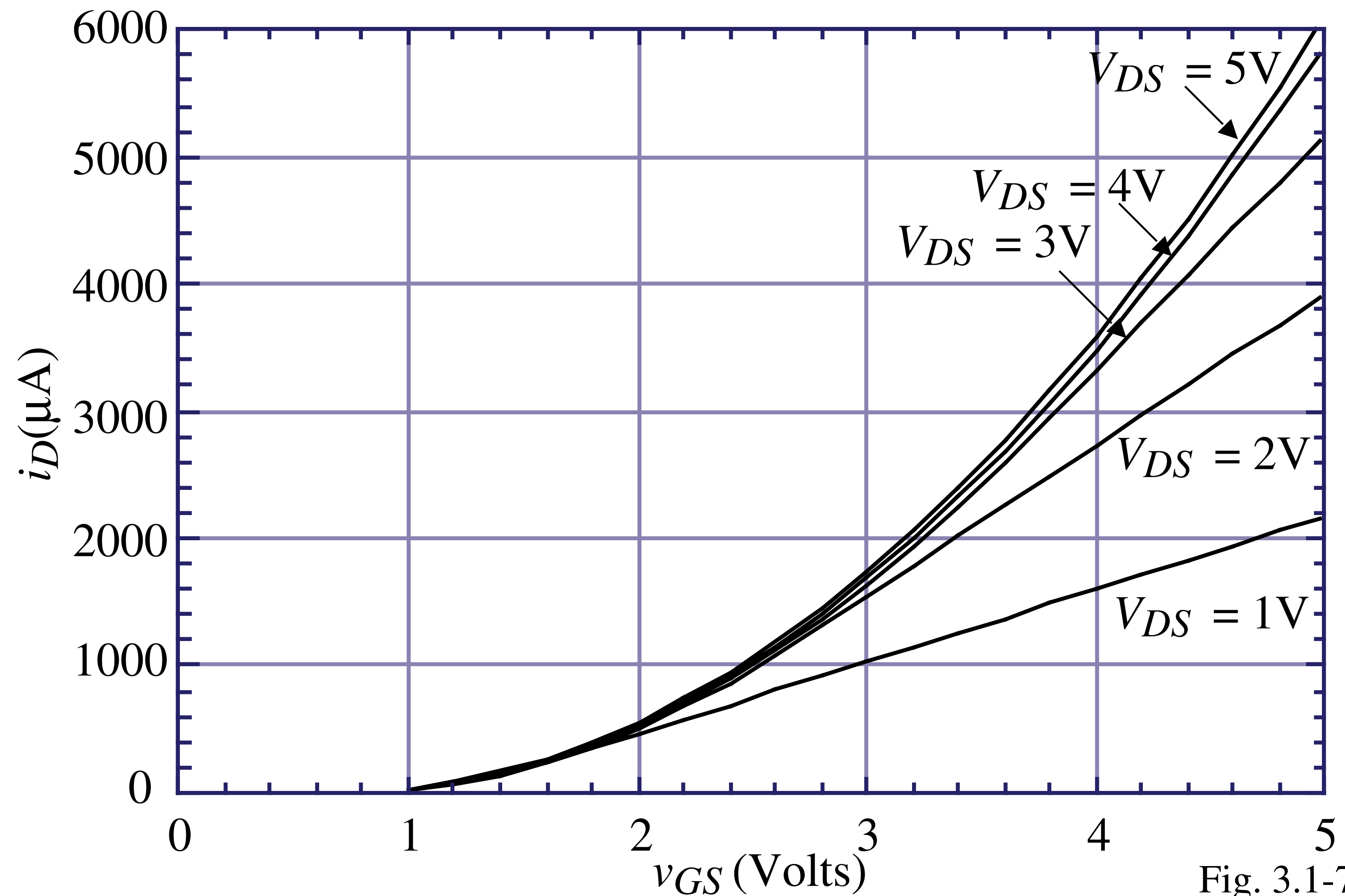

Fig. 3.1-7

SPICE Input File:

```
Transconductance Characteristics for NMOS
M1 1 6 0 0 MOS1 w=5u l=1.0u
VDS1 1 0 1.0
M2 2 6 0 0 MOS1 w=5u l=1.0u
VDS2 2 0 2.0
M3 3 6 0 0 MOS1 w=5u l=1.0u
VDS3 3 0 3.0
M4 4 6 0 0 MOS1 w=5u l=1.0u
VDS4 4 0 4.0
M5 5 6 0 0 MOS1 w=5u l=1.0u
VDS5 5 0 5.0
VGS 6 0 5
.model mos1 nmos (vto=0.7 kp=110u
+gamma=0.4 lambda=.04 phi=.7)
.dc vgs 0 5 .2
.print dc ID(M1), ID(M2), ID(M3), ID(M4),
ID(M5)
.probe
.end
```

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3.2 - LARGE SIGNAL FET MODEL FOR HAND CALCULATIONS

Large Signal Model Derivation

Derivation-

1.) Let the charge per unit area in the channel inversion layer be

$$Q_I(y) = -C_{ox}[v_{GS}-v(y)-V_T] \quad (\text{coul./cm}^2)$$

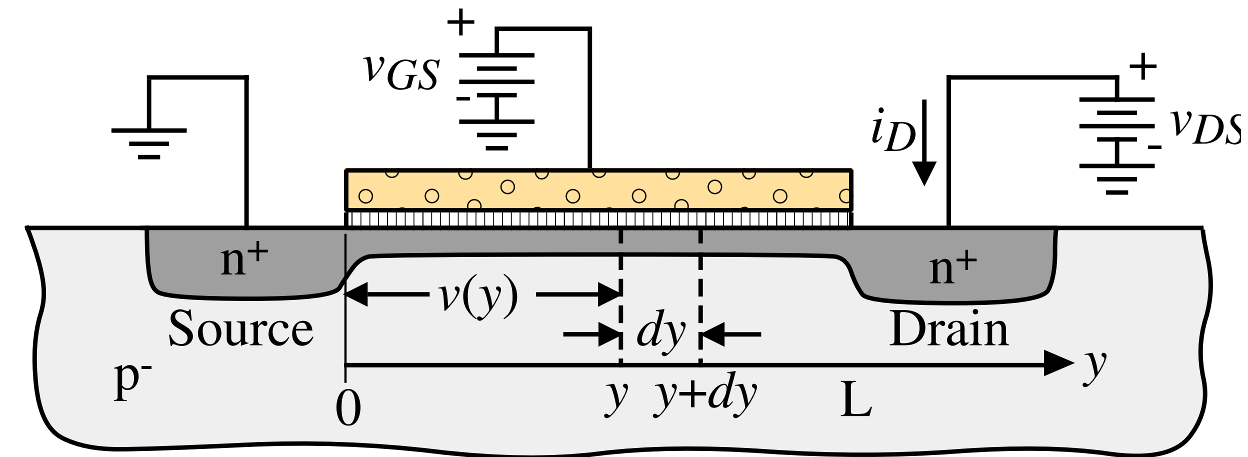

Fig.110-03

2.) Define sheet conductivity of the inversion layer per square as

$$\sigma_S = \mu_o Q_I(y) \quad \left(\frac{\text{cm}^2}{\text{v·s}}\right)\left(\frac{\text{coulombs}}{\text{cm}^2}\right) = \frac{\text{amps}}{\text{volt}} = \frac{1}{\Omega/\text{sq.}}$$

3.) Ohm's Law for current in a sheet is

$$J_S = \frac{i_D}{W} = -\sigma_S E_y = -\sigma_S \frac{dv}{dy} \rightarrow \quad dv = \frac{-i_D}{\sigma_S W}\, dy = \frac{-i_D dy}{\mu_o Q_I(y) W} \rightarrow \quad i_D\, dy = -W\mu_o Q_I(y) dv$$

4.) Integrating along the channel for 0 to L gives

$$\int_0^L i_D dy = -\int_0^{v_{DS}} W\mu_o Q_I(y) dv = \int_0^{v_{DS}} W\mu_o C_{ox}[v_{GS}-v(y)-V_T]\, dv$$

5.) Evaluating the limits gives

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS}-V_T)v(y) - \frac{v^2(y)}{2}\right]_0^{v_{DS}} \rightarrow \quad \boxed{i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS}-V_T)v_{DS} - \frac{v_{DS}^2}{2}\right]}$$

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Saturation Voltage - V_{DS}(sat)

Interpretation of the large signal model:

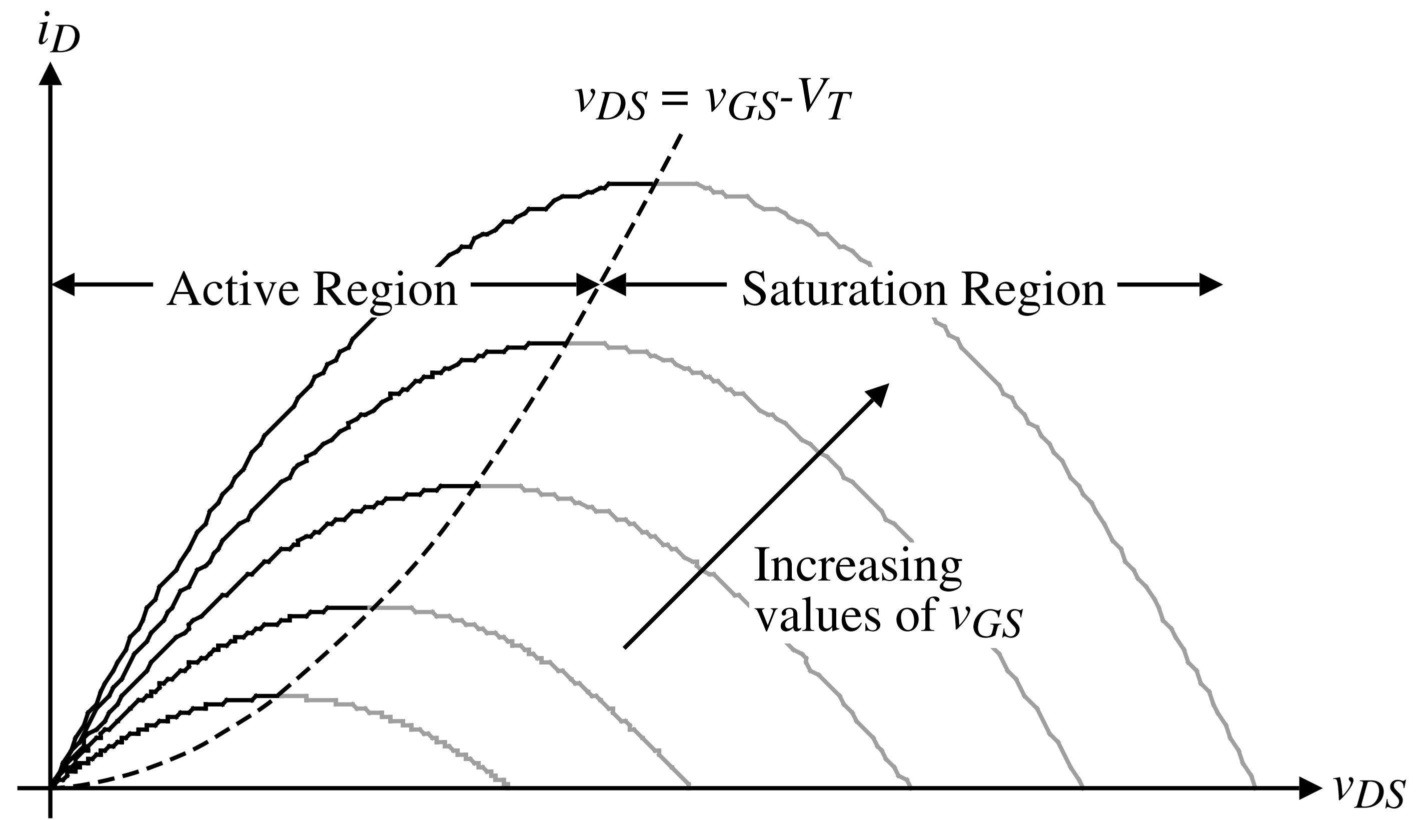

Fig. 110-04

The saturation voltage for MOSFETs is the value of drain-source voltage at the peak of the inverted parabolas.

$$\frac{di_D}{dv_{DS}} = \frac{\mu_o C_{ox} W}{L}[(v_{GS}-V_T) - v_{DS}] = 0$$

$$\boxed{v_{DS}(\text{sat}) = v_{GS} - V_T}$$

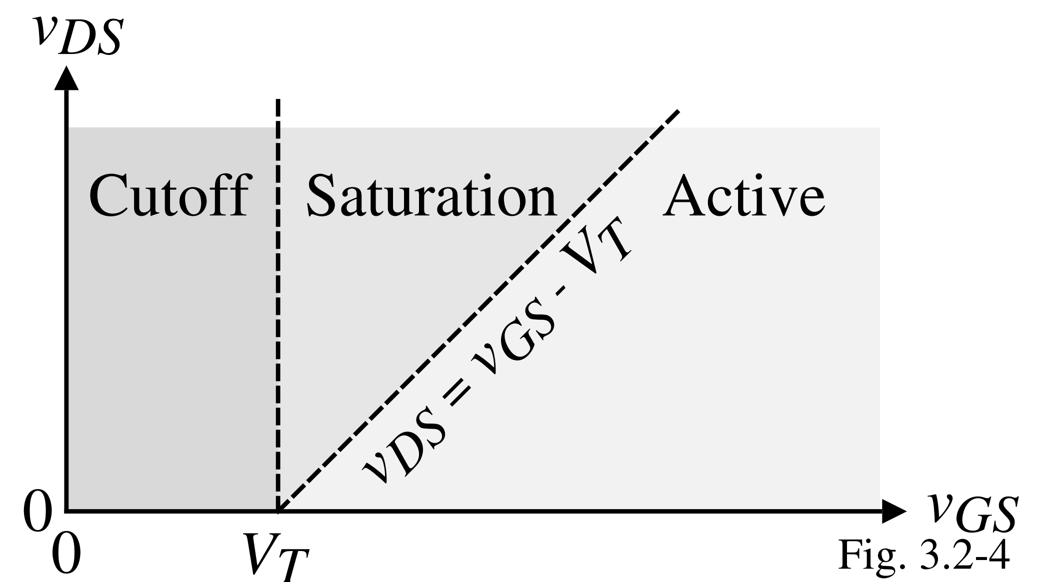

Fig. 3.2-4

Useful definitions:

$$\frac{\mu_o C_{ox} W}{L} = \frac{K'W}{L} = \beta$$

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The Simple Large Signal MOSFET Model

Regions of Operation of the MOS Transistor:

1.) Cutoff Region:

$$v_{GS} - V_T < 0$$

$$i_D = 0$$

(Ignores subthreshold currents)

2.) Active Region

$$0 < v_{DS} < v_{GS} - V_T$$

$$i_D = \frac{\mu_o C_{ox} W}{2L}\left[2(v_{GS} - V_T) - v_{DS}\right] v_{DS}$$

3.) Saturation Region

$$0 < v_{GS} - V_T < v_{DS}$$

$$i_D = \frac{\mu_o C_{ox} W}{2L}\left(v_{GS} - V_T\right)^2$$

Output Characteristics of the MOSFET:

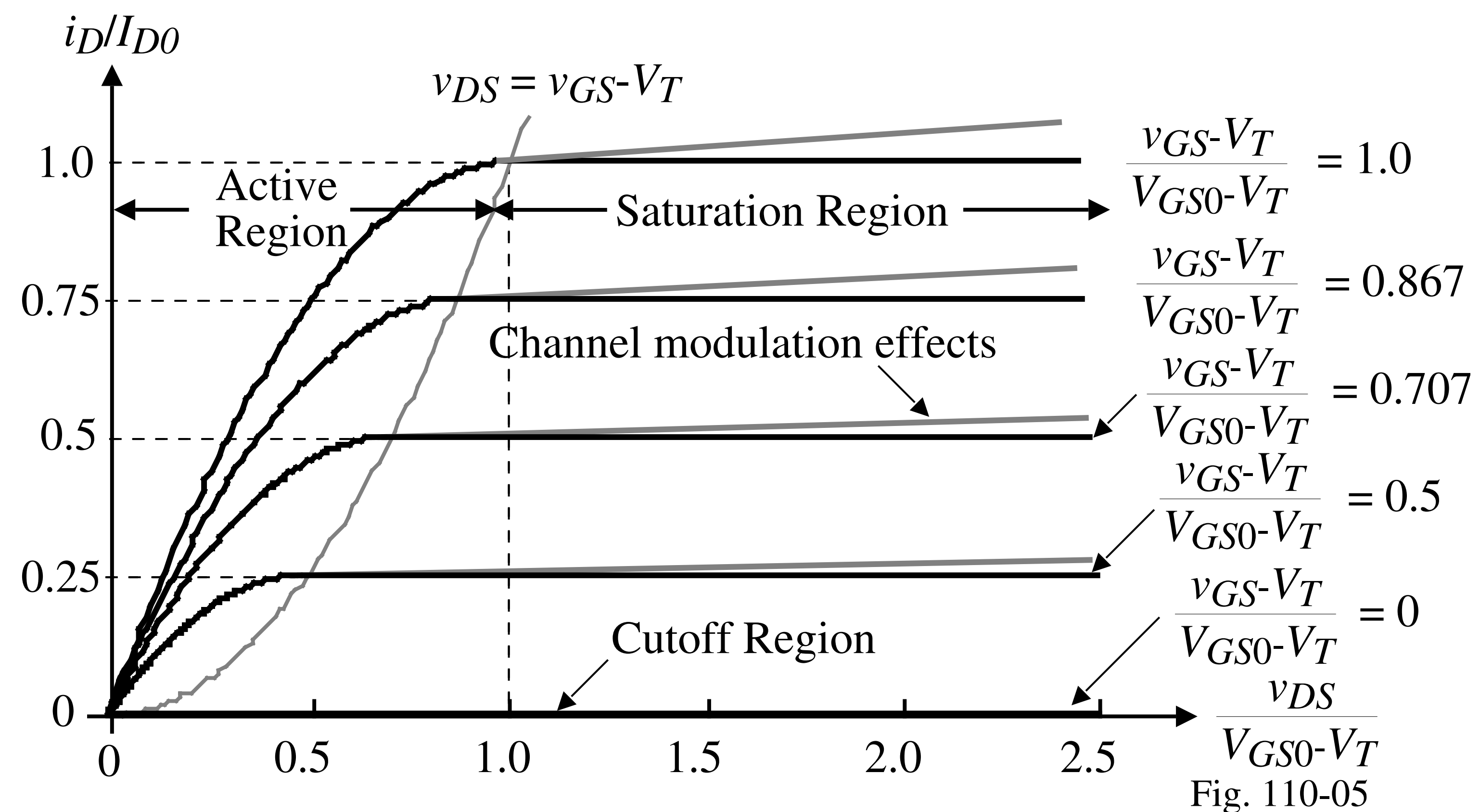

Fig. 110-05

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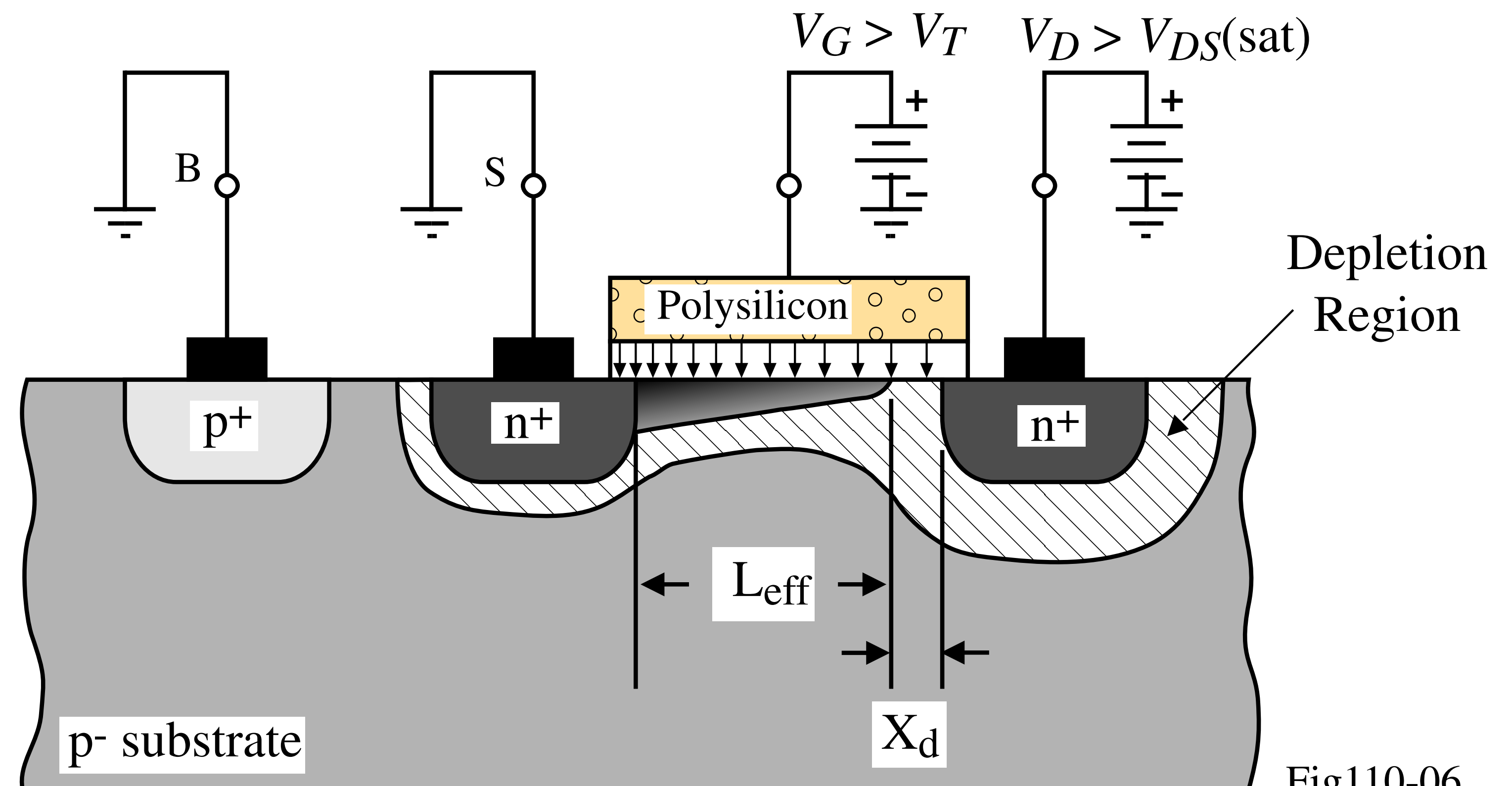
Influence of V_{DS} on the Output Characteristics

Channel modulation effect:

As the value of v_{DS} increases, the effective L decreases causing the current to increase.

Illustration:



Note that $L_{eff} = L - X_d$

Therefore the model in saturation becomes,

$$i_D = \frac{K'W}{2L_{eff}}(v_{GS}-V_T)^2 \;\rightarrow\; \frac{di_D}{dv_{DS}} = -\frac{K'W}{2L_{eff}^2}(v_{GS}-V_T)^2\frac{dL_{eff}}{dv_{DS}} = \frac{i_D}{L_{eff}}\frac{dX_d}{dv_{DS}} \equiv \lambda i_D$$

Therefore, a good approximation to the influence of v_{DS} on i_D is

$$i_D \approx i_D(\lambda = 0) + \frac{di_D}{dv_{DS}}v_{DS} = i_D(\lambda = 0)(1 + \lambda v_D) = \frac{K'W}{2L}(v_{GS}-V_T)^2(1+\lambda v_{DS})$$

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Channel Length Modulation Parameter, λ

Assume the MOS is transistor is saturated-

$$\therefore \quad i_D = \frac{\mu C_{ox} W}{2L}(v_{GS} - V_T)^2(1 + \lambda v_{DS})$$

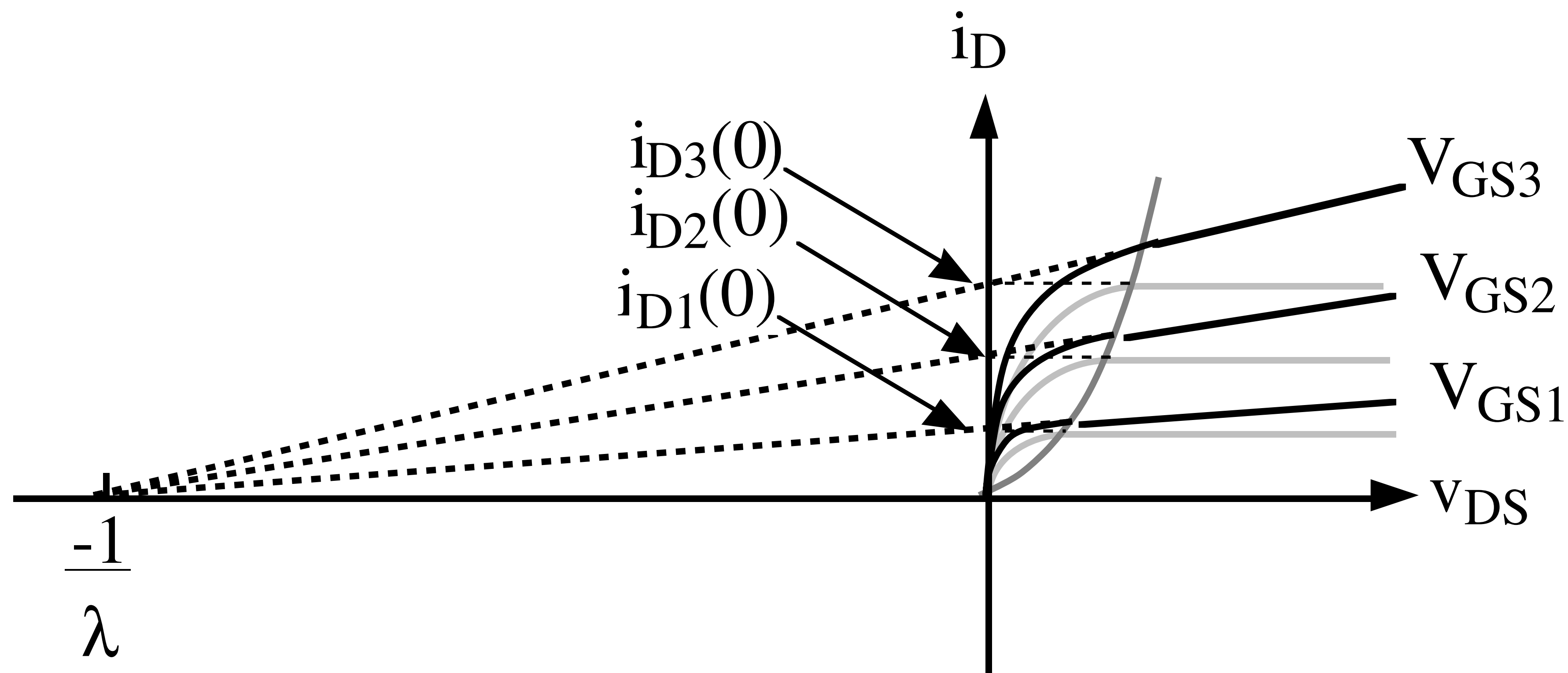
Define $i_D(0) = i_D$ when $v_{DS} = 0\text{V}$.

$$\therefore \quad i_D(0) = \frac{\mu C_{ox} W}{2L}(v_{GS} - V_T)^2$$

Now,

$$i_D = i_D(0)[1 + \lambda v_{DS}] = i_D(0) + \lambda i_D(0)\, v_{DS}$$

Matching with $y = mx + b$ gives the value of λ



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Influence of the Bulk Voltage on the Large Signal MOSFET Model

Illustration of the influence of the bulk:

$V_{SB0} = 0V$:

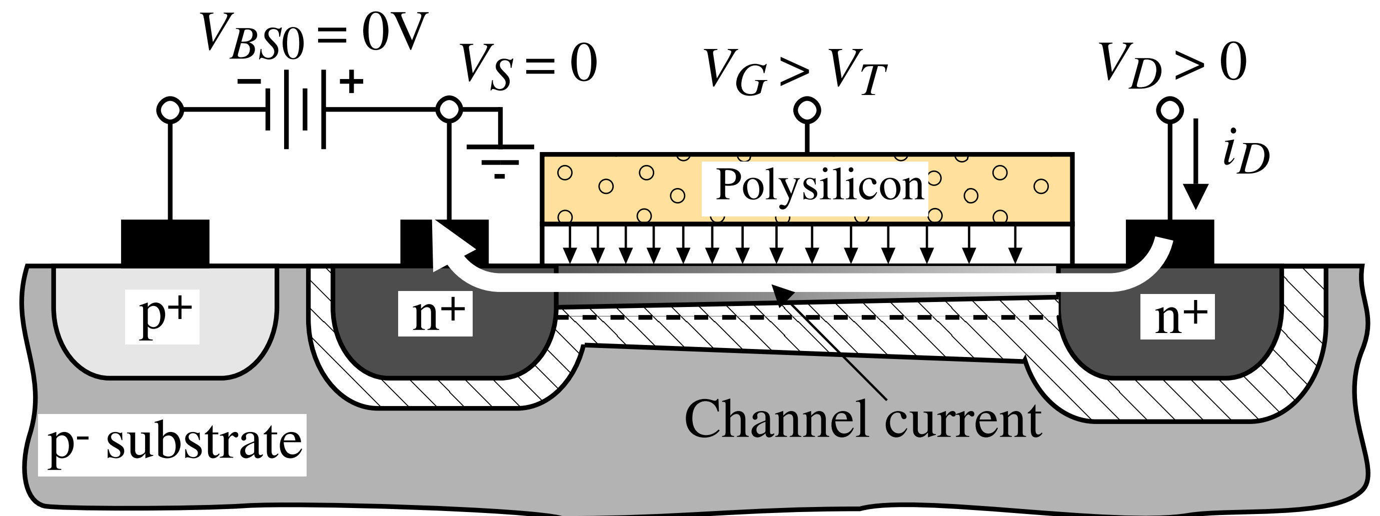

Fig.110-07A

$V_{SB1}>0V$:

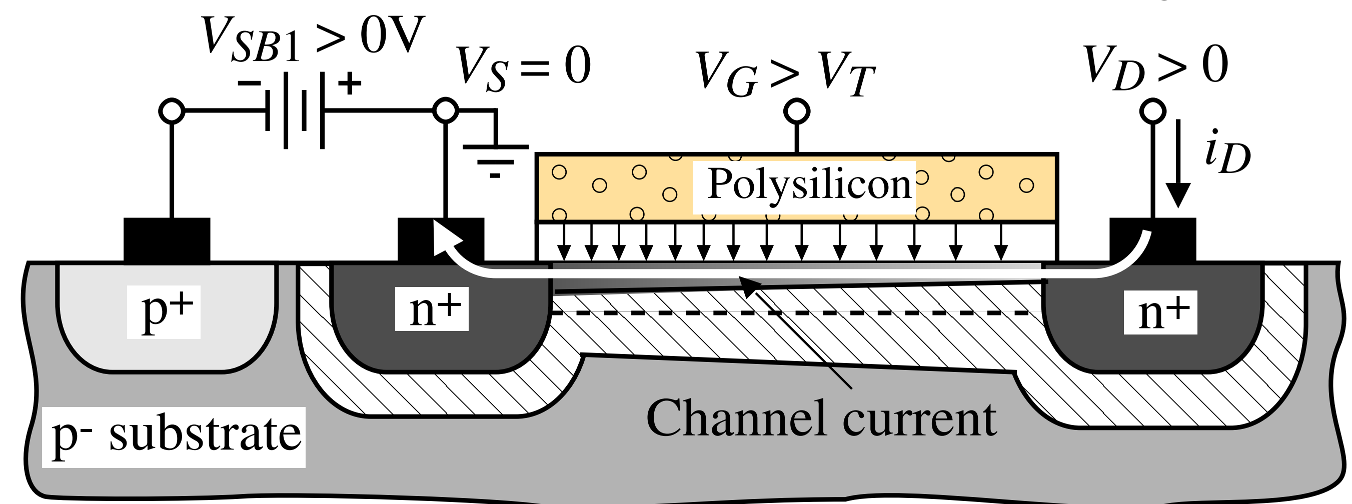

Fig.110-07B

$V_{SB2} > V_{SB1}$:

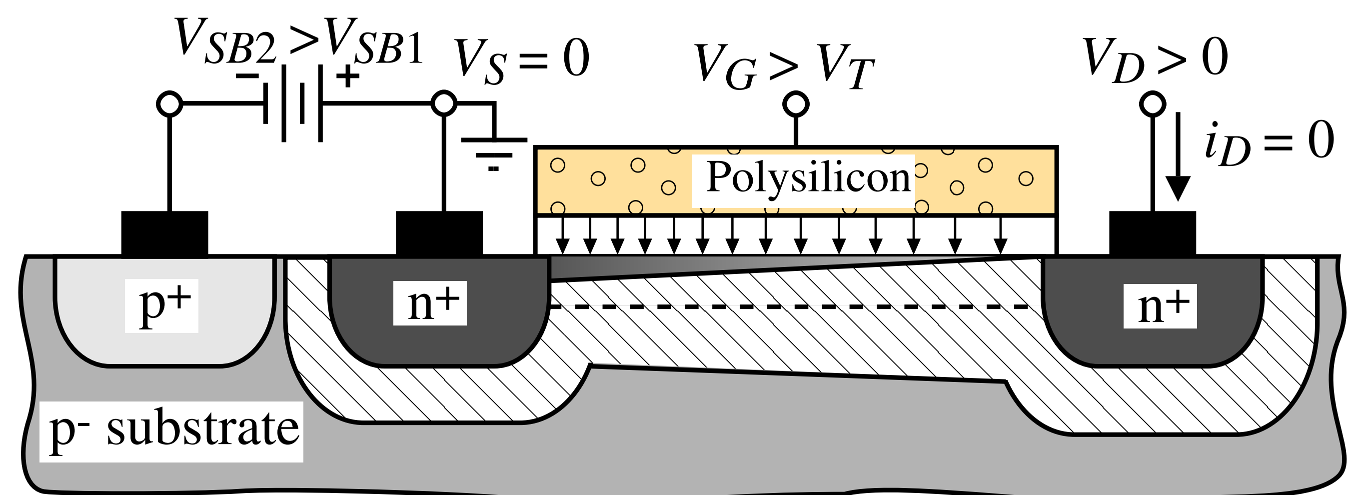

Fig.110-07C

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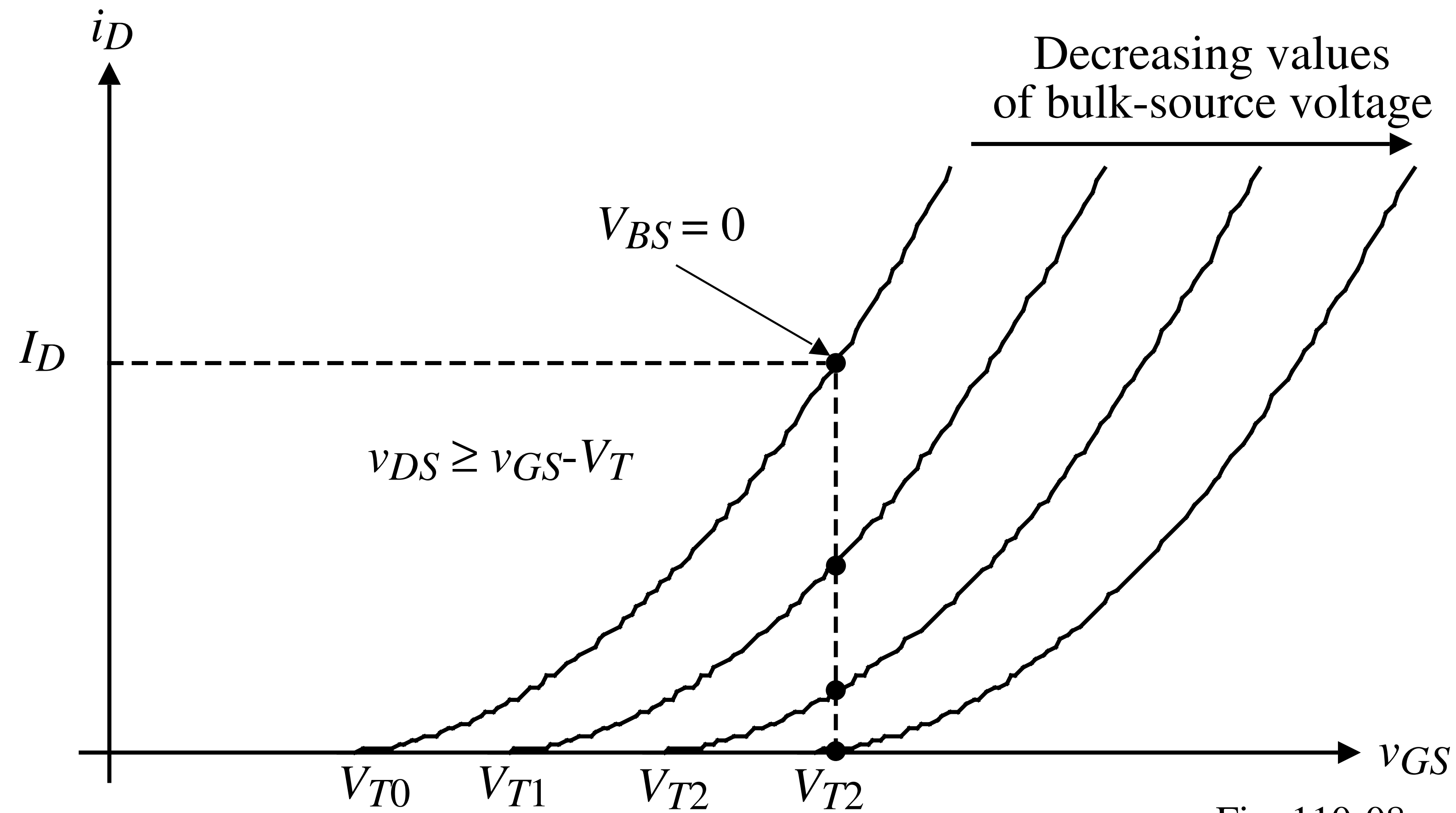
Influence of the Bulk Voltage on the Large Signal MOSFET Model - Continued

Bulk-Source (v_{BS}) influence on the transconductance characteristics-



In general, the simple model incorporates the bulk effect into V_T by the previously developed relationship:

$$V_T(v_{BS}) = V_{T0} + \gamma\sqrt{2|\phi_f| + |v_{BS}|} - \gamma\sqrt{2|\phi_f|}$$

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Summary of the Simple Large Signal MOSFET Model

N-channel reference convention:

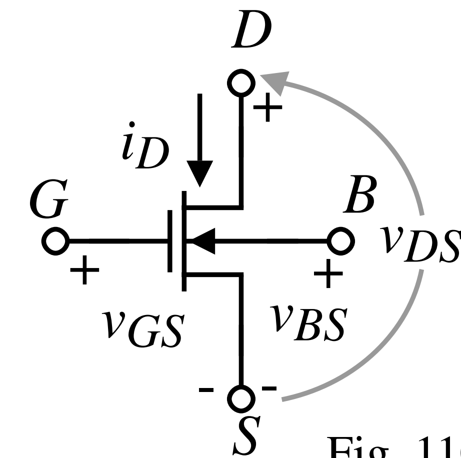

Fig. 110-10

Non-saturation-

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right](1 + \lambda v_{DS})$$

Saturation-

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS}-V_T)v_{DS}(\text{sat}) - \frac{v_{DS}(\text{sat})^2}{2}\right](1+\lambda v_{DS}) = \frac{W\mu_o C_{ox}}{2L}(v_{GS}-V_T)^2(1+\lambda v_{DS})$$

where:

μ_o = zero field mobility (cm^2/volt·sec)

C_{ox} = gate oxide capacitance per unit area (F/cm^2)

λ = channel-length modulation parameter ($volts^{-1}$)

$$V_T = V_{T0} + \gamma\left(\sqrt{2|\phi_f| + |v_{BS}|} - \sqrt{2|\phi_f|}\right)$$

V_{T0} = zero bias threshold voltage

γ = bulk threshold parameter ($volts^{-0.5}$)

$2|\phi_f|$ = strong inversion surface potential (volts)

For p-channel MOSFETs, use n-channel equations with p-channel parameters and invert current.

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Silicon Constants

Constant Symbol	Constant Description	Value	Units
V_G	Silicon bandgap (27°C)	1.205	V
k	Boltzmann's constant	1.381×10^{-23}	J/K
n_i	Intrinsic carrier concentration (27°C)	1.45×10^{10}	cm^{-3}
ε_0	Permittivity of free space	8.854×10^{-14}	F/cm
ε_{si}	Permittivity of silicon	$11.7\ \varepsilon_0$	F/cm
ε_{ox}	Permittivity of SiO_2	$3.9\ \varepsilon_0$	F/cm

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MOSFET Parameters

Model Parameters for a Typical CMOS Bulk Process (0.8μm CMOS n-well):

Parameter Symbol	Parameter Description	Typical Parameter Value		
		N-Channel	P-Channel	Units
$VT0$	Threshold Voltage ($V_{BS} = 0$)	0.7± 0.15	-0.7 ± 0.15	V
K'	Transconductance Parameter (in saturation)	110.0 ± 10%	50.0 ± 10%	$\mu A/V^2$
γ	Bulk threshold parameter	0.4	0.57	$(V)^{1/2}$
λ	Channel length modulation parameter	0.04 (L=1 μm) 0.01 (L=2 μm)	0.05 (L=1 μm) 0.01 (L=2 μm)	$(V)^{-1}$
$2\|\phi F\|$	Surface potential at strong inversion	0.7	0.8	V

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3.3 - LARGE SIGNAL MODEL EXTENSIONS TO SHORT-CHANNEL MOSFETS

Extensions

- Velocity saturation
- Weak inversion (subthreshold)
- Substrate currents

Substrate Interference

- Problems of mixed signal circuits on the same substrate
- Modeling and potential solutions

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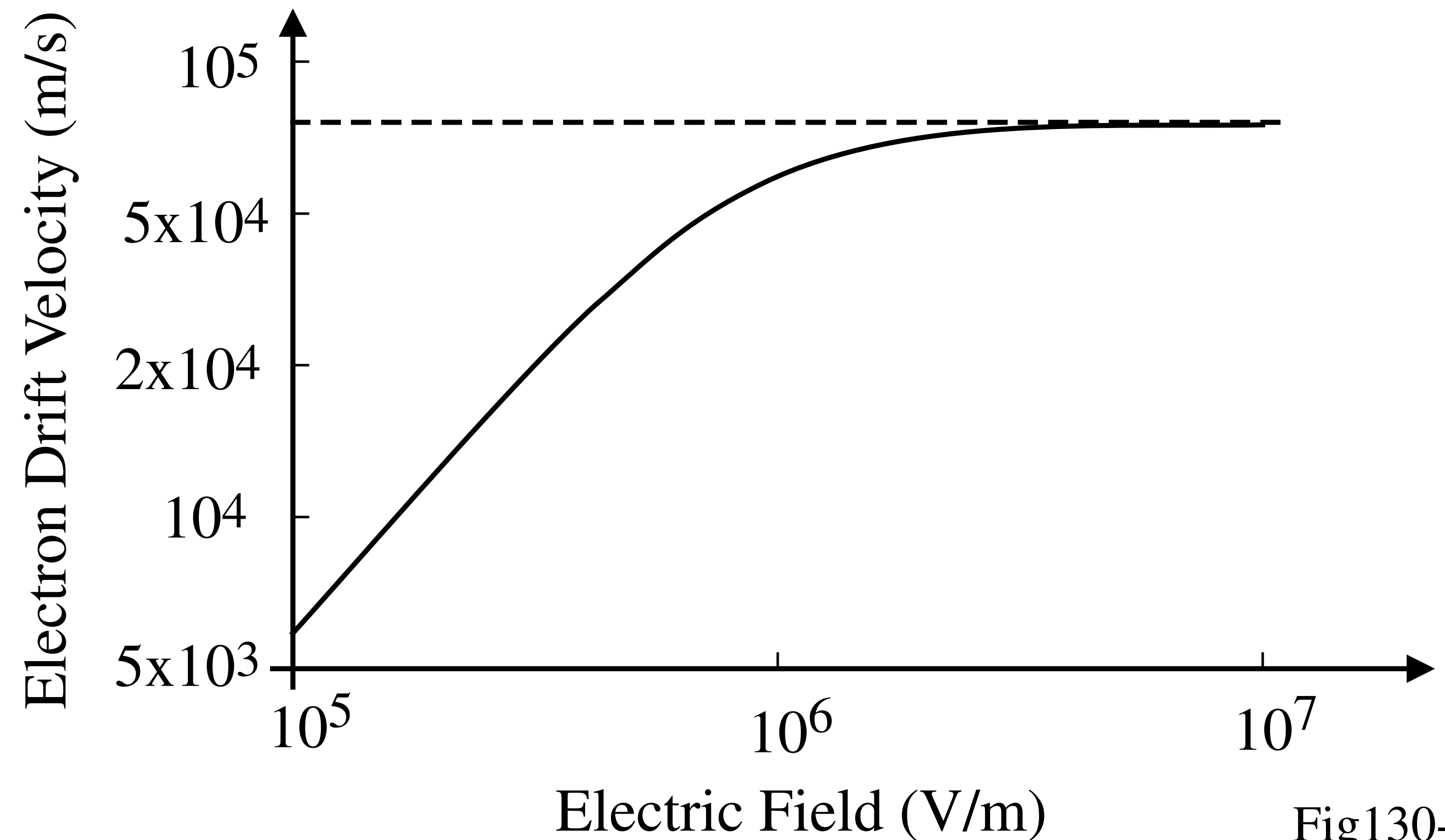
VELOCITY SATURATION

What is Velocity Saturation?

The most important short-channel effect in MOSFETs is the velocity saturation of carriers in the channel. A plot of electron drift velocity versus electric field is shown below.



An expression for the electron drift velocity as a function of the electric field is,

$$v_d \approx \frac{\mu_n E}{1 + E/E_c}$$

where

v_d = electron drift velocity (m/s)

μ_n = low-field mobility ($\approx 0.07\text{m}^2/\text{V}\cdot\text{s}$)

E_c = critical electrical field at which velocity saturation occurs

Important Short Channel Effects

1.) An approximate plot of the n as a function of channel length is shown below where

$$i_D \propto (v_{GS} - V_T)^n$$

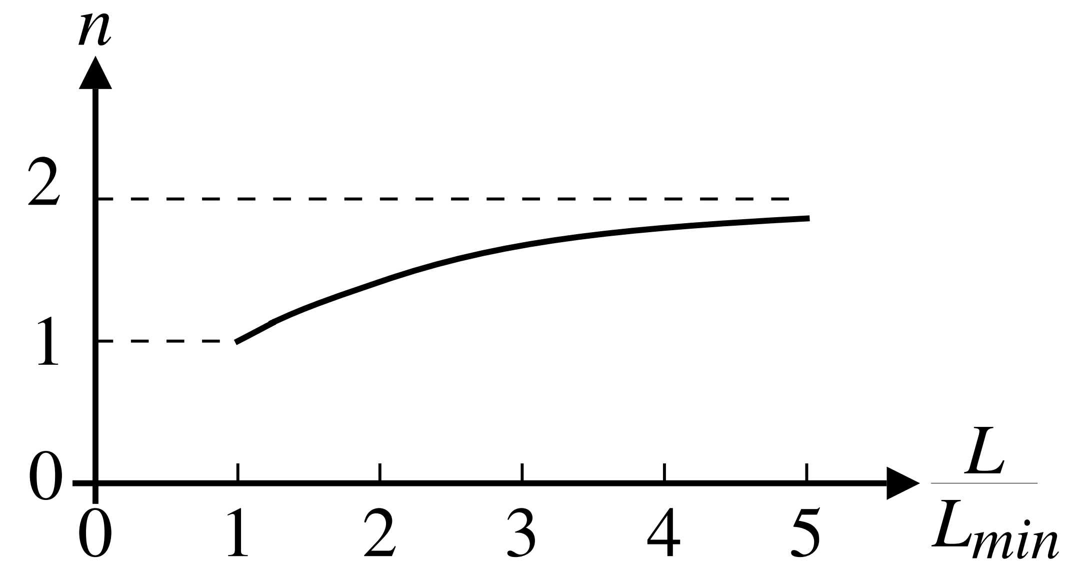


Fig.130-5

2.) Note that the value of λ varies with channel length, L. The data below is from a 0.25µm CMOS technology.

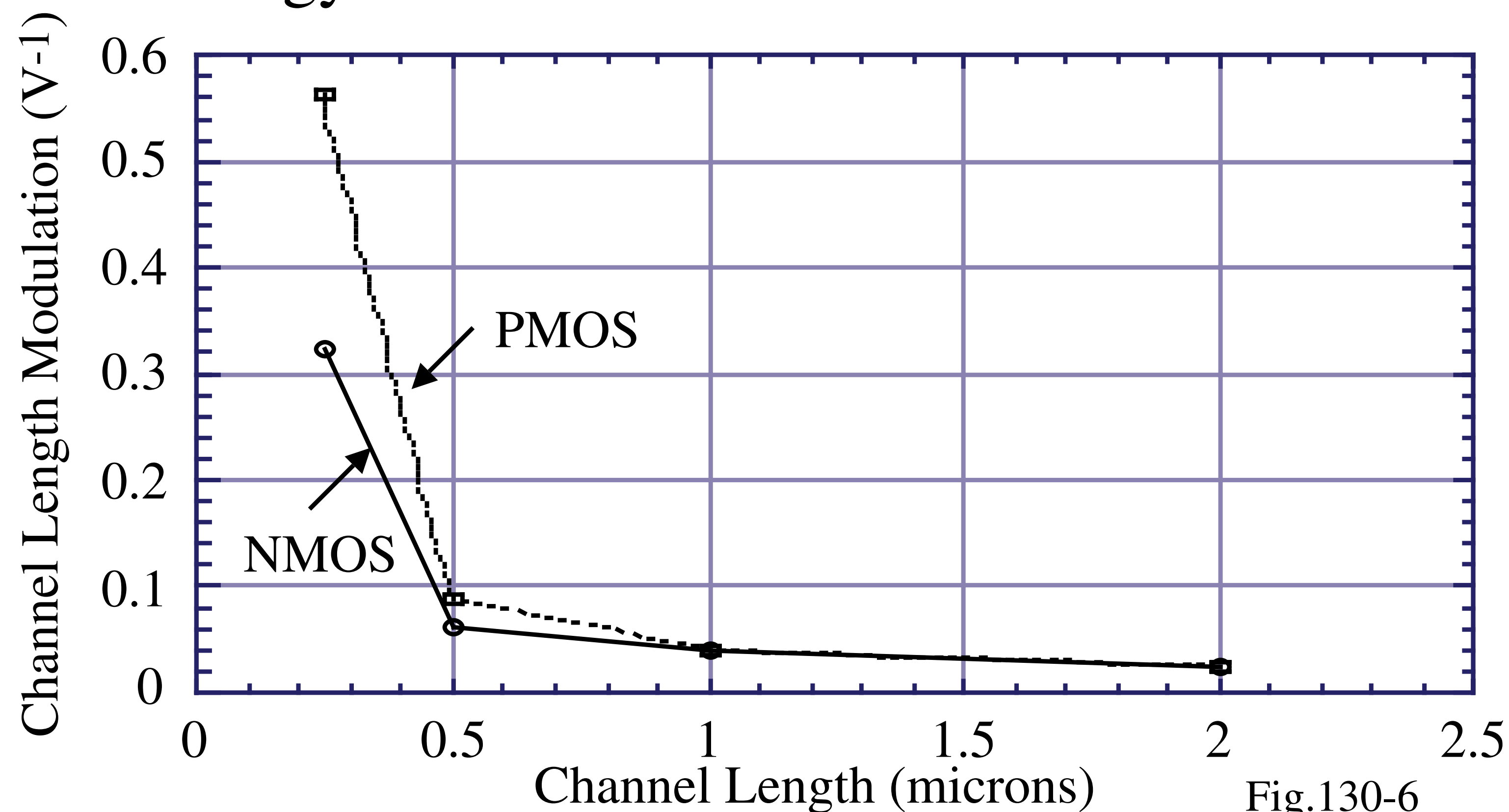


Fig.130-6

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SUBTHRESHOLD MOSFET MODEL

What is Weak Inversion Operation?

Weak inversion operation occurs when the applied gate voltage is below V_T and pertains to when the surface of the substrate beneath the gate is weakly inverted.

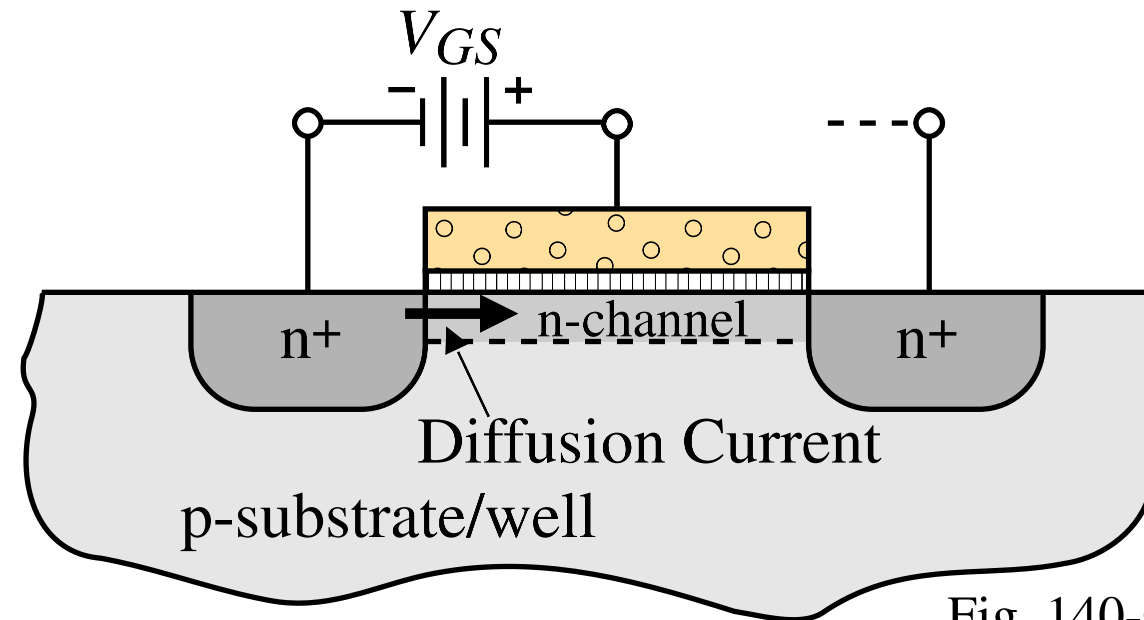

Fig. 140-01

Regions of operation according to the surface potential, ϕ_S (or ψ_S)

$\phi_S < \phi_F$:	Substrate not inverted
$\phi_F < \phi_S < 2\phi_F$:	Channel is weakly inverted (diffusion current)
$2\phi_F < \phi_S$:	Strong inversion (drift current)

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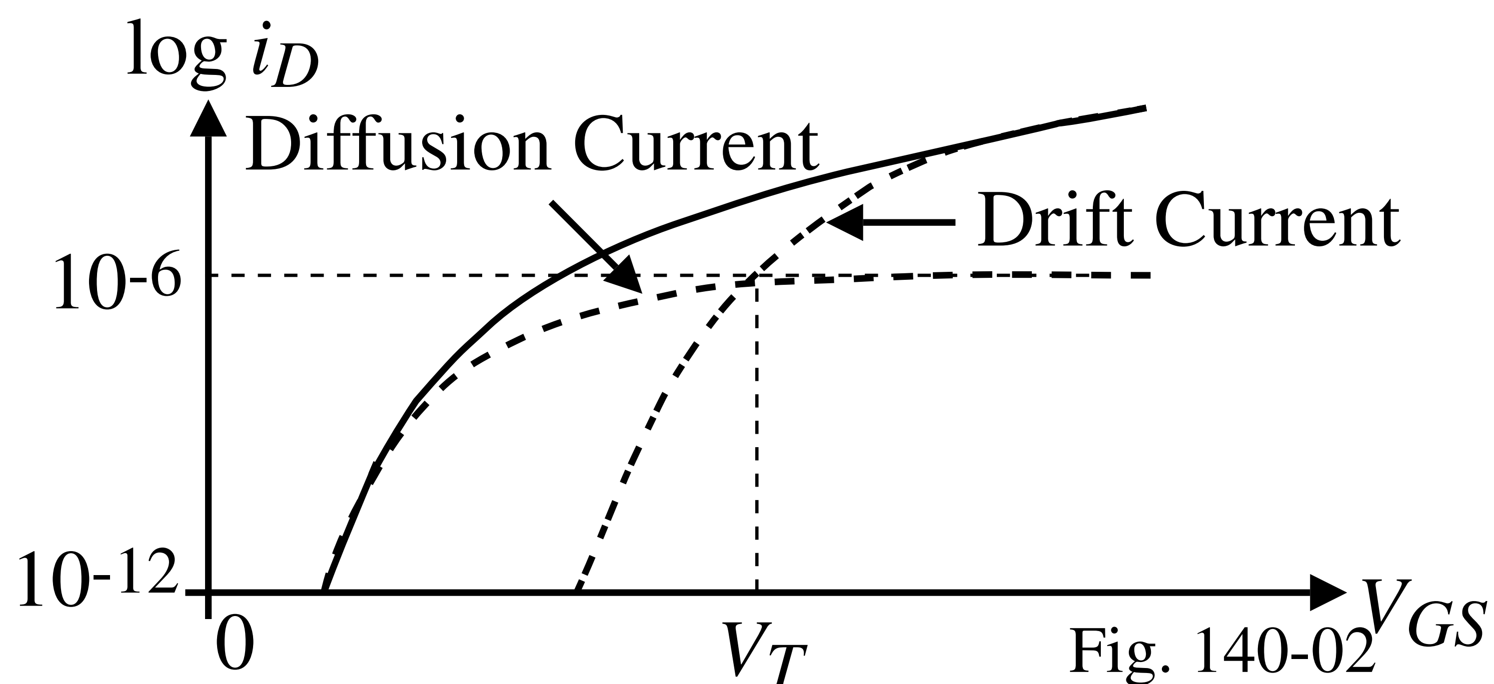
Drift versus Diffusion Current

1.) For strong inversion, the gate voltage controls the charge in the inverted region but not in the depletion region. The concentration of charge across the channel is approximately constant and the current is drift caused by electric field.

2.) For weak inversion, the charge in channel is much less that that in the depletion region and drift current decreases. However, there is a concentration gradient in the channel, that causes diffusion current.

The n-channel MOSFET acts like a NPN BJT: the emitter is the source, the base is the substrate and the collector is the drain.

Illustration:



Simulation of an n-channel MOSFET in both Weak and Strong Inversion

Uses the BSIM model.†

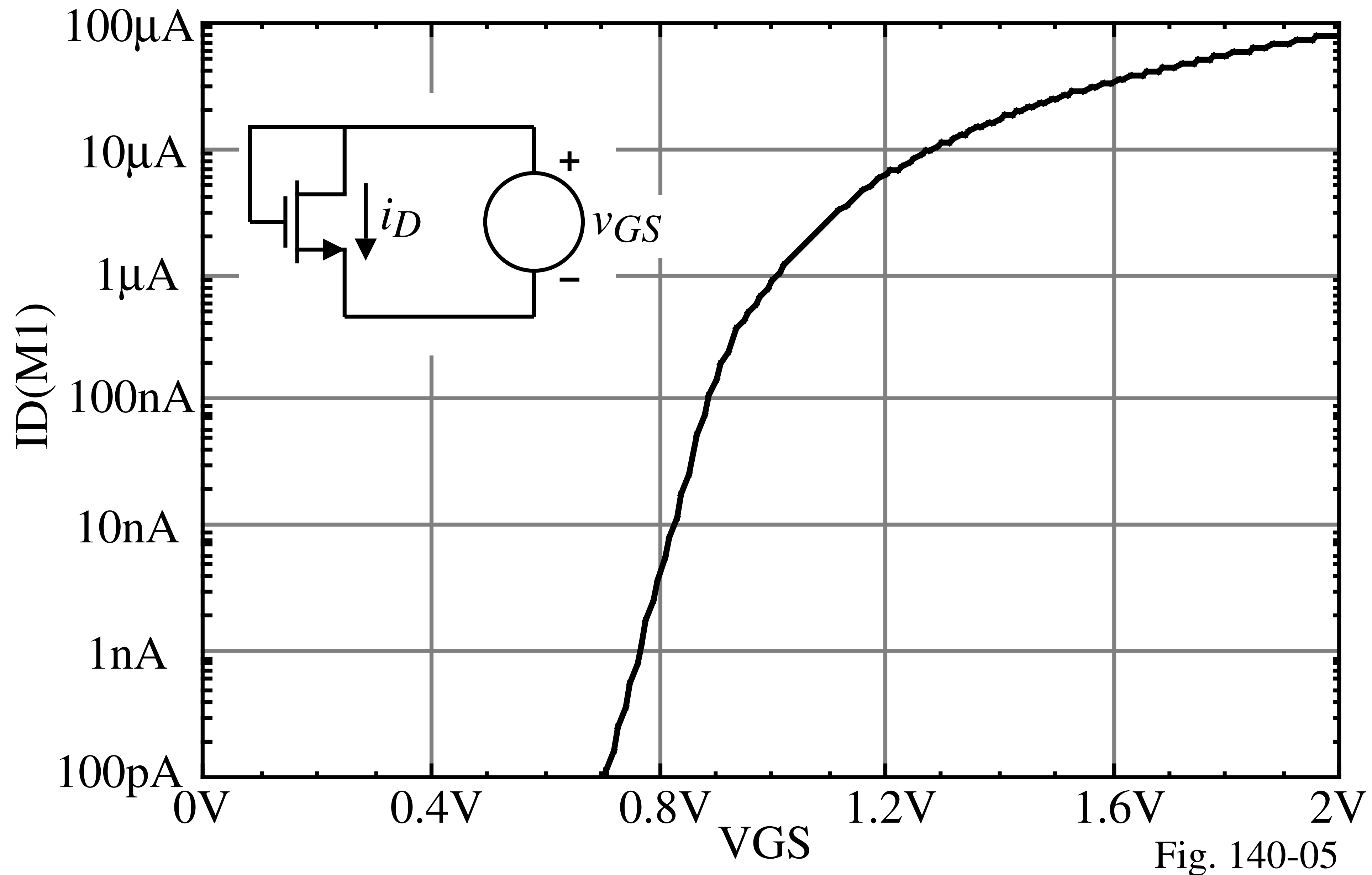


Fig. 140-05

† Y. Cheng and C. Hu, *MOSFET Modeling & BSIM3 User's Guide*, Kluwer Academic Publishers, Boston, 1999.

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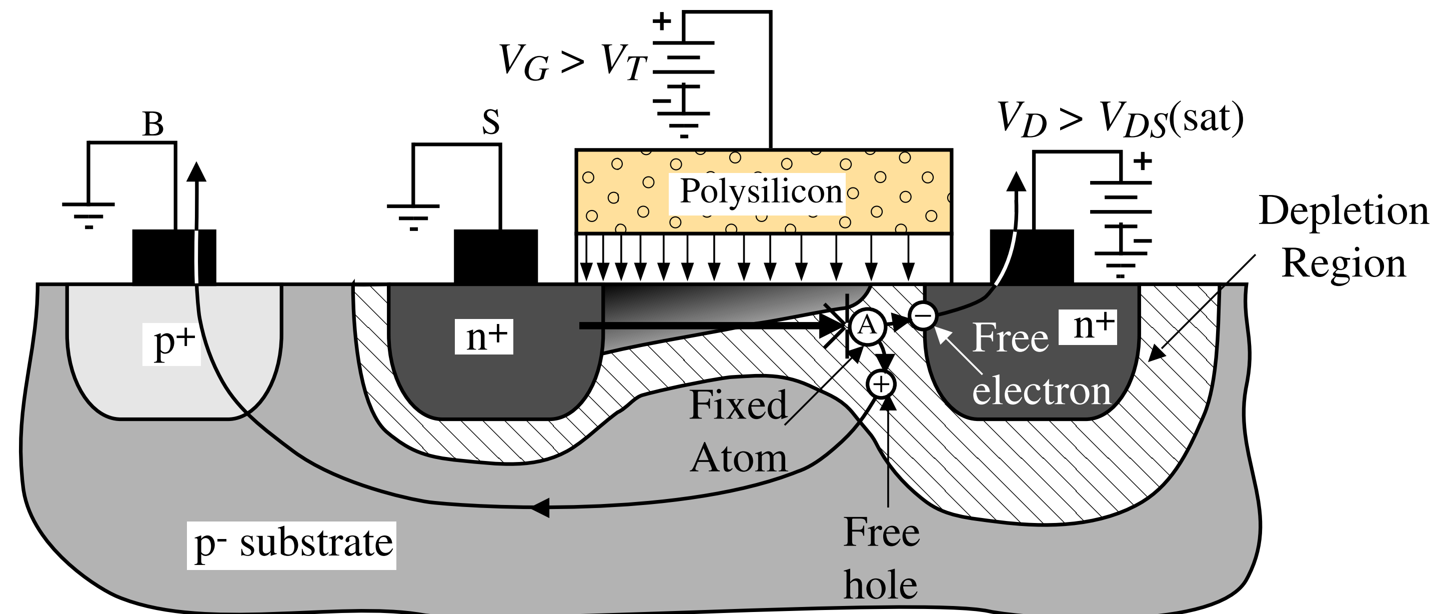
SUBSTRATE CURRENT FLOW IN MOSFETS

Impact Ionization

Impact Ionization:

Occurs because high electric fields cause an impact which generates a hole-electron pair. The electrons flow out the drain and the holes flow into the substrate causing a substrate current flow.

Illustration:



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SUBSTRATE INTERFERENCE IN CMOS CIRCUITS

How Do Carriers Get Injected into the Substrate?

1.) Hot carriers (substrate current)

2.) Electrostatic coupling (across depletion regions and other dielectrics)

3.) Electromagnetic coupling (parallel conductors)

Why is this a Problem?

With decreasing channel lengths, more circuitry is being integrated on the same substrate. The result is that noisy circuits (circuits with rapid transitions) are beginning to adversely influence sensitive circuits (such as analog circuits).

Present Solution

Keep circuit separate by using multiple substrates and put the multiple substrates in the same package.

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Hot Carrier Injection in CMOS Technology without an Epitaxial Region

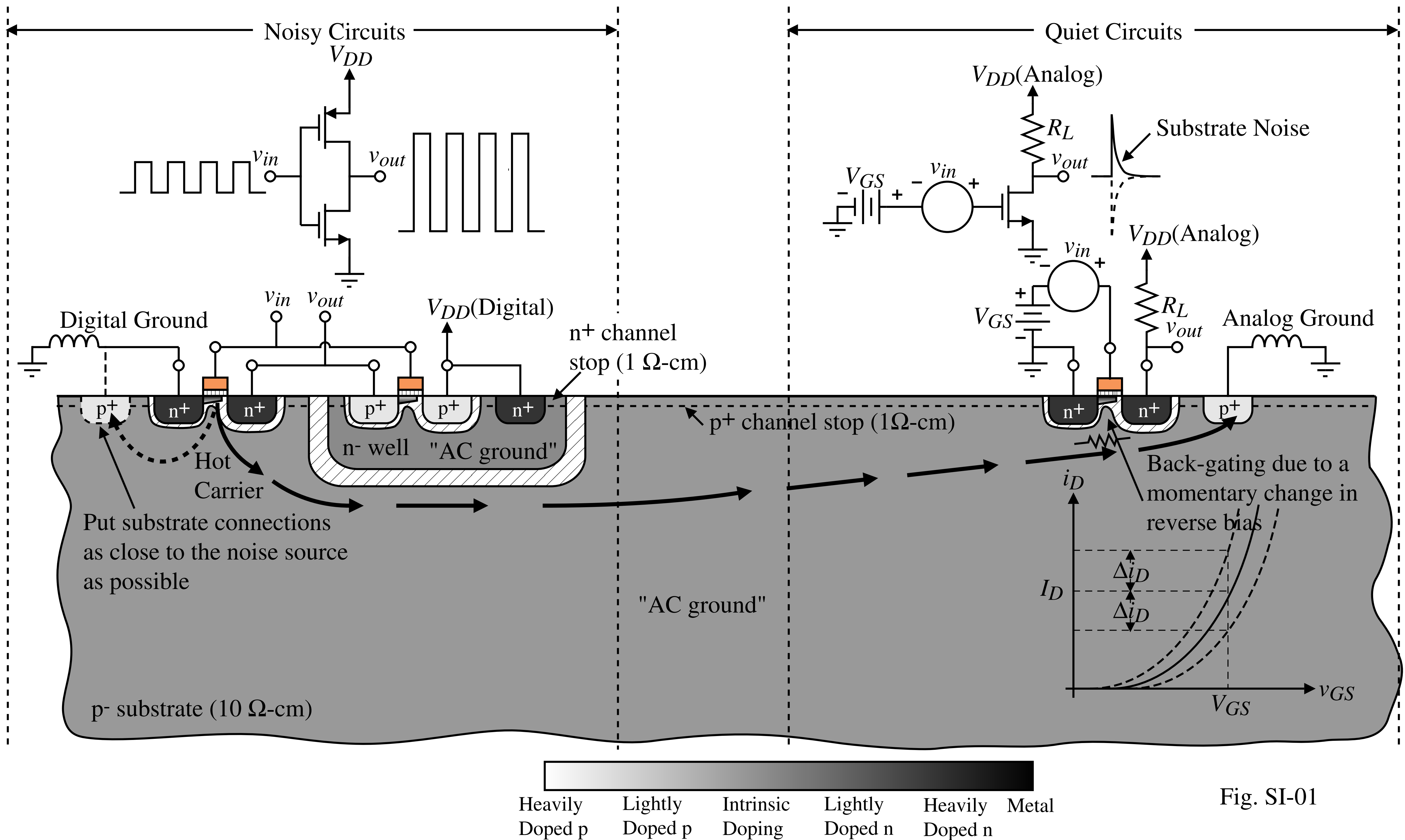

Fig. SI-01

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Hot Carrier Injection in CMOS Technology with an Epitaxial Region

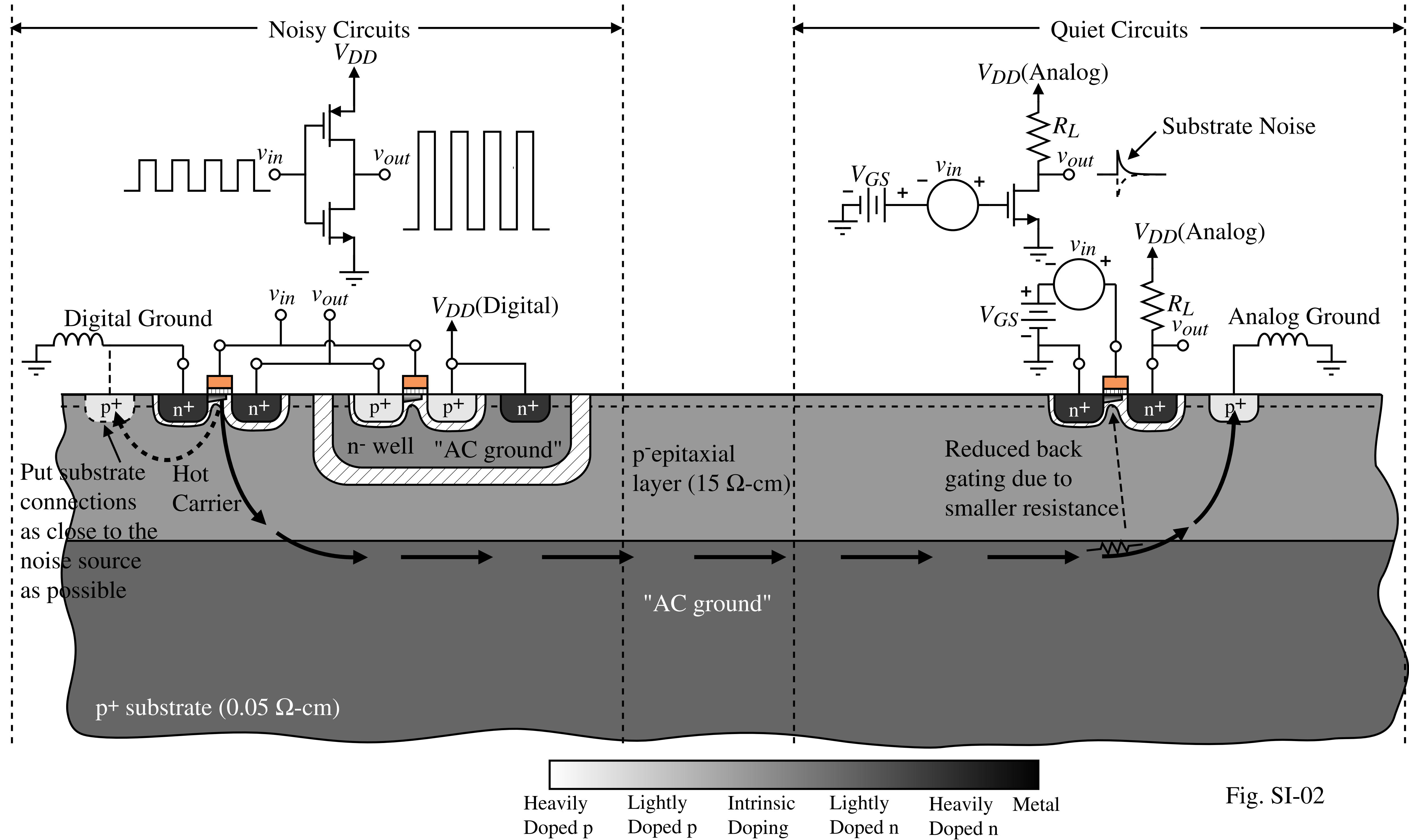

Fig. SI-02

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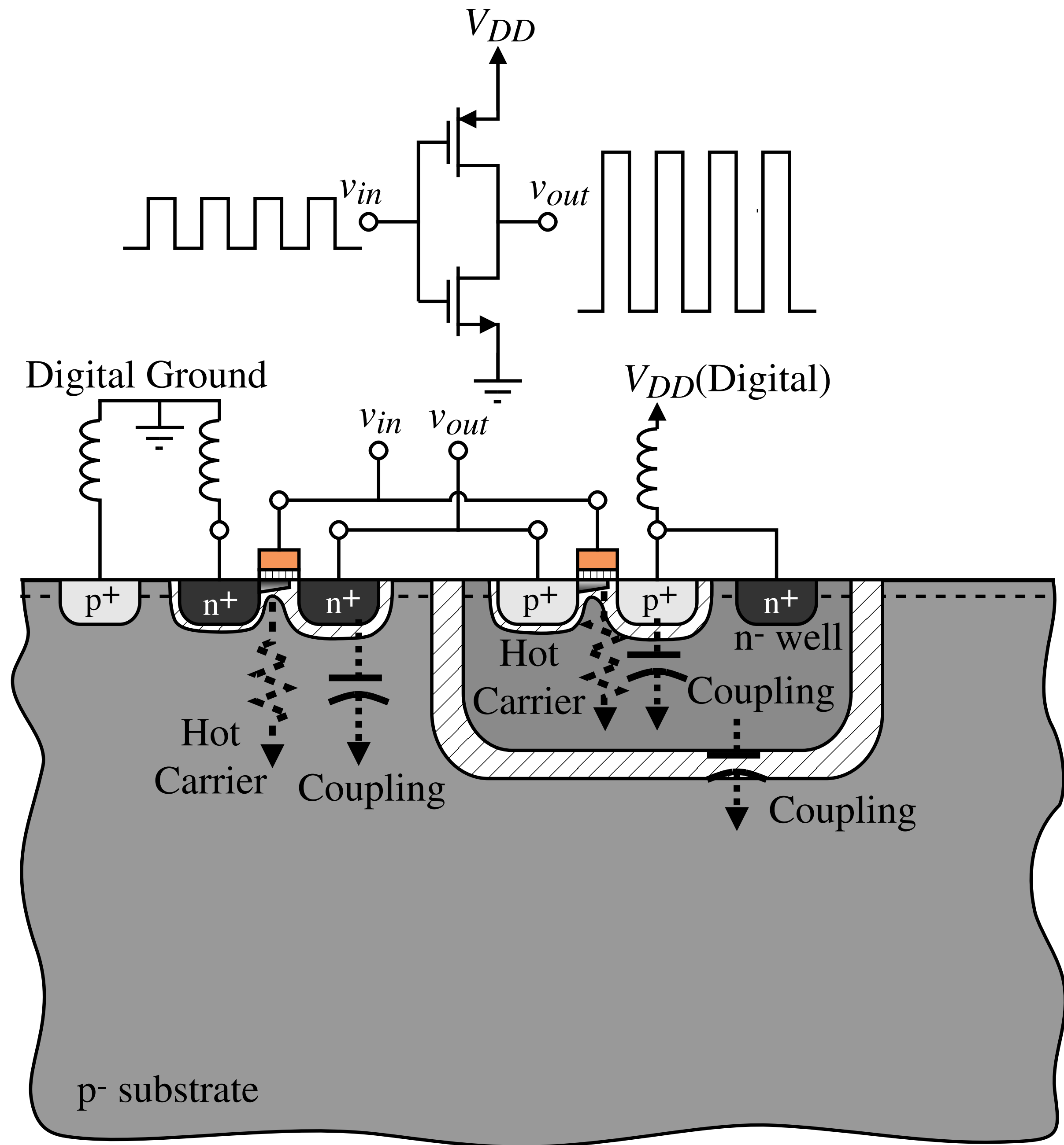
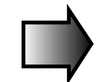
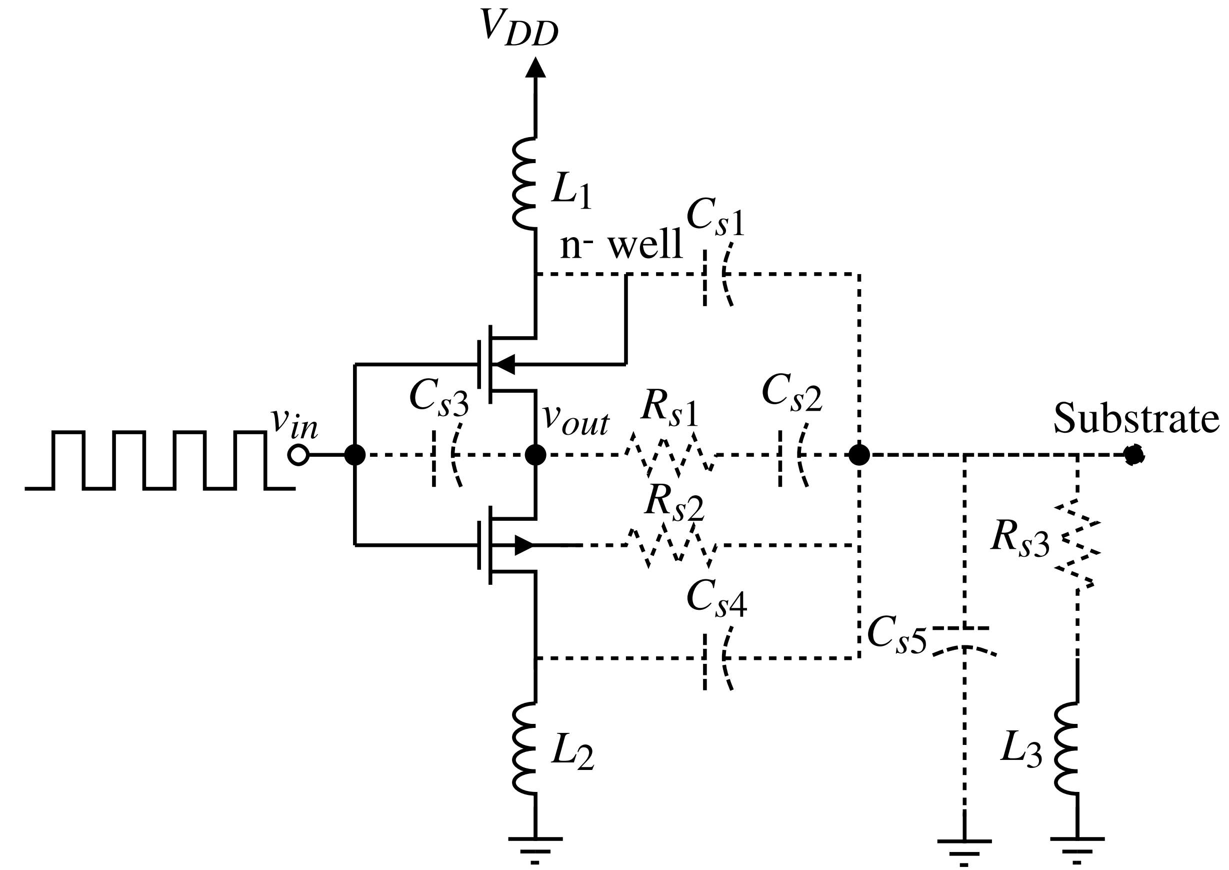
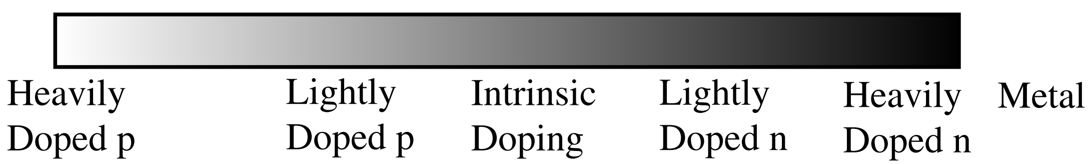
Computer Model for Substrate Interference Using SPICE Primitives

Noise Injection Model:









C_{s1} = Capacitance between n-well and substrate

C_{s2},C_{s3} and C_{s4} = Capacitances between interconnect lines (including bond pads) and substrate

C_{s5} = All capacitance between the substrate and ac ground

R_{s1},R_{s2} and R_{s3} = Bulk resistances in n-well and substrate

L_1,L_2 and L_3 = Inductance of the bond wires and package leads

Fig. SI-06

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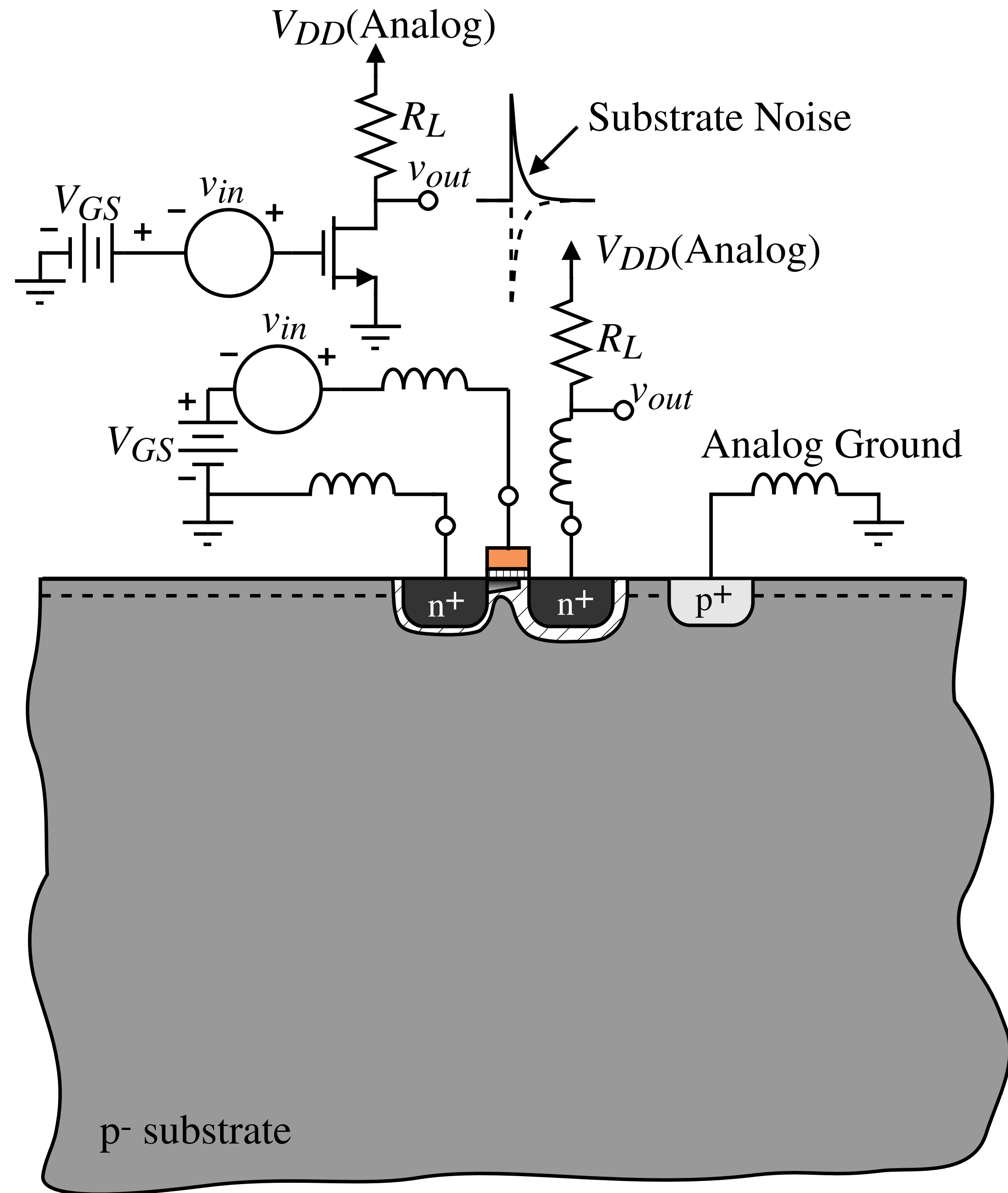
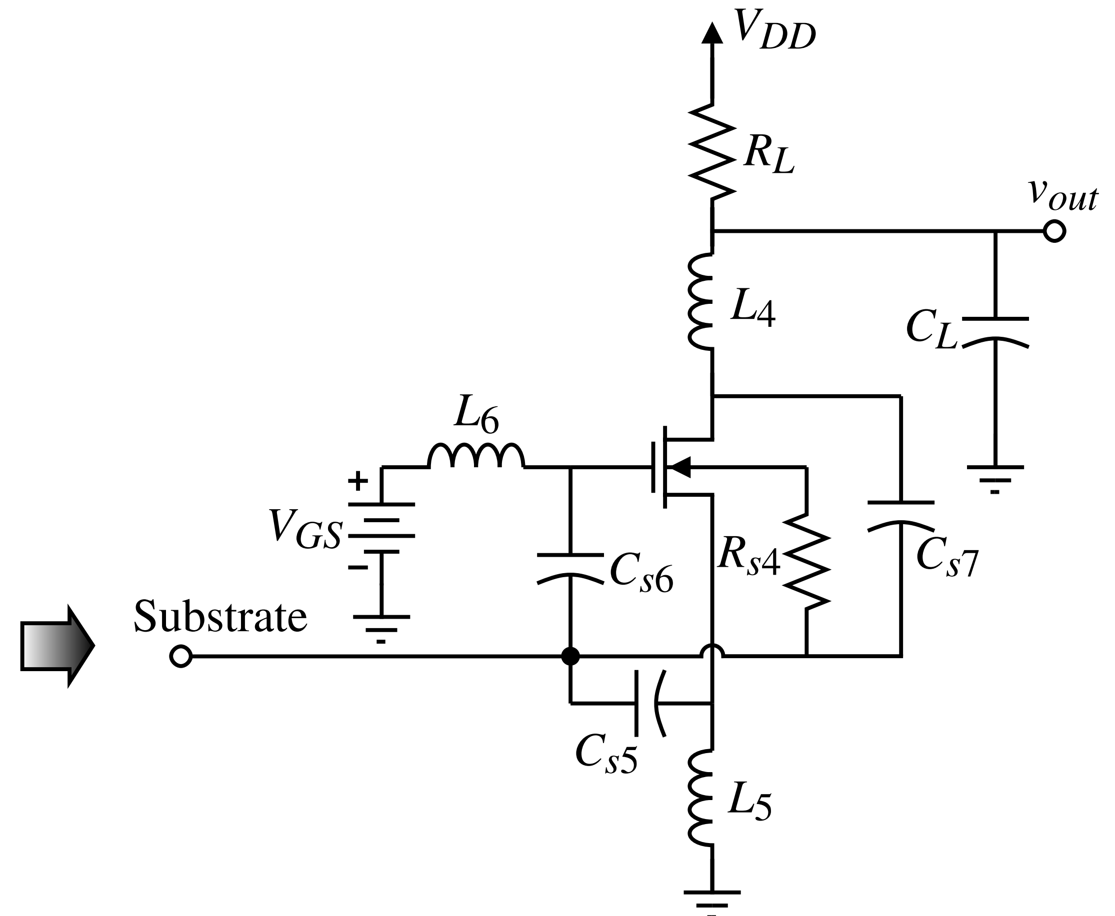
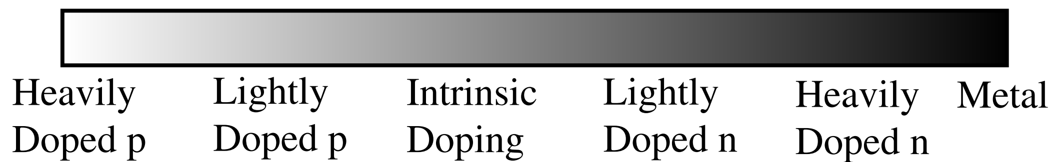
Computer Model for Substrate Interference Using SPICE Primitives

Noise Detection Model:







C_{s5},C_{s6} and C_{s7} = Capacitances between interconnect lines (including bond pads) and substrate

R_{s4} = Bulk resistance in the substrate

L_4,L_5 and L_6 = Inductance of the bond wires and package leads

Fig. SI-07

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Other Sources of Substrate Injection

(We do it to ourselves and can’t blame the digital circuits.)

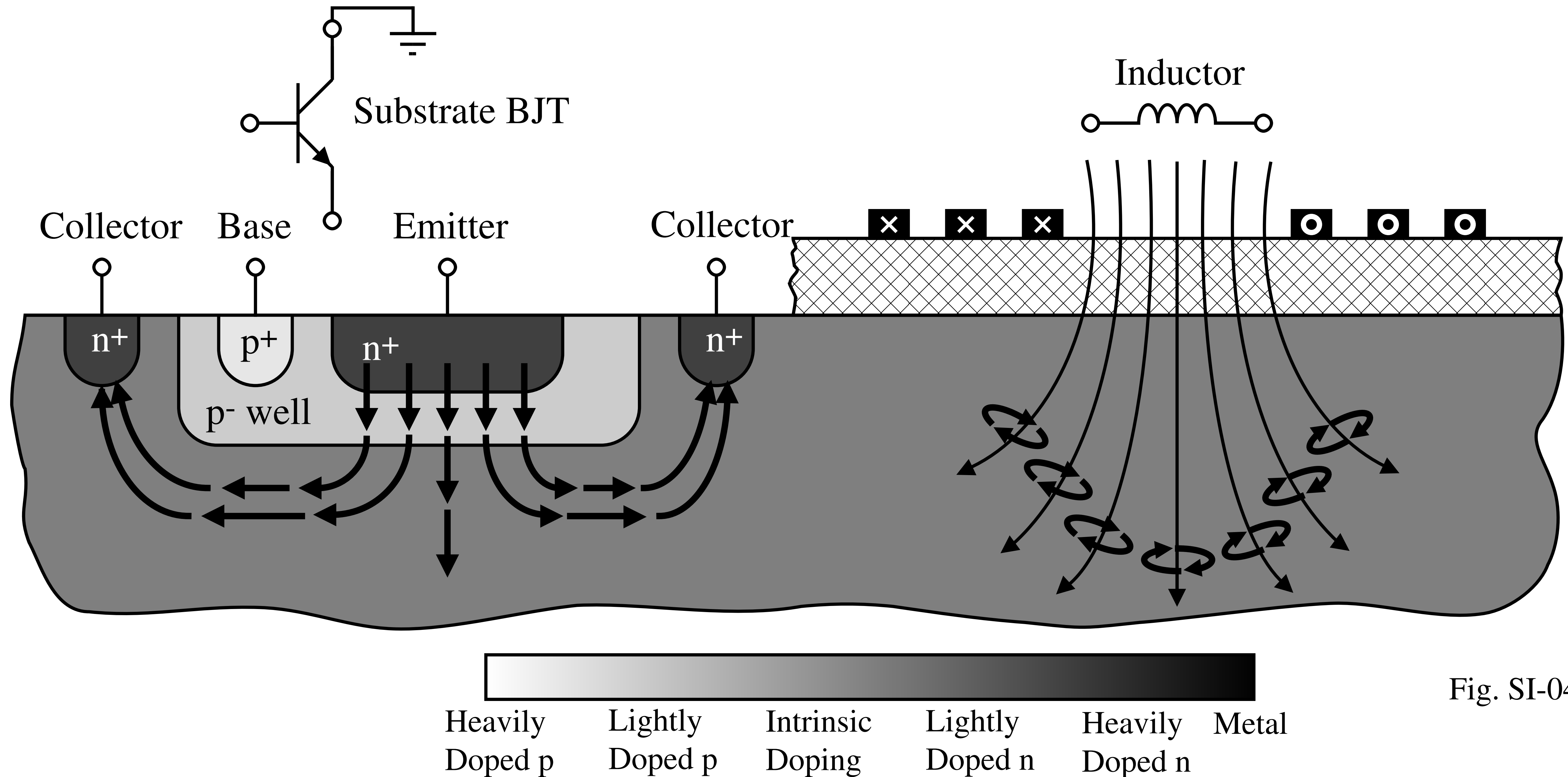

Fig. SI-04

Also, there is coupling from power supplies and clock lines to other adjacent signal lines.

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What is a Good Ground?

- On-chip, it is a region with very low bulk resistance.

  It is best accomplished by connecting metal to the region at as many points as possible.

- Off-chip, it is all determined by the connections or bond wires.

  The inductance of the bond wires is large enough to create significant ground potential changes for fast current transients.

$$v = L\frac{di}{dt}$$

  Use multiple bonding wires to reduce the ground noise caused by inductance.

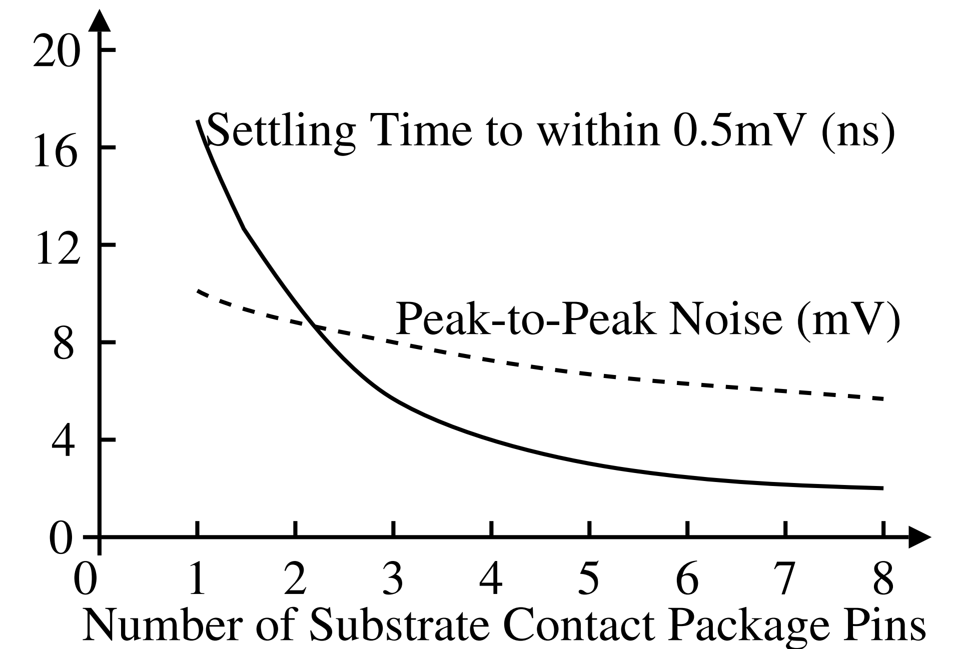

Fig. SI-08

- Fast changing signals have part of their path (circuit through ground and power supplies. Therefore bypass the off-chip power supplies to ground as close to the chip as possible.

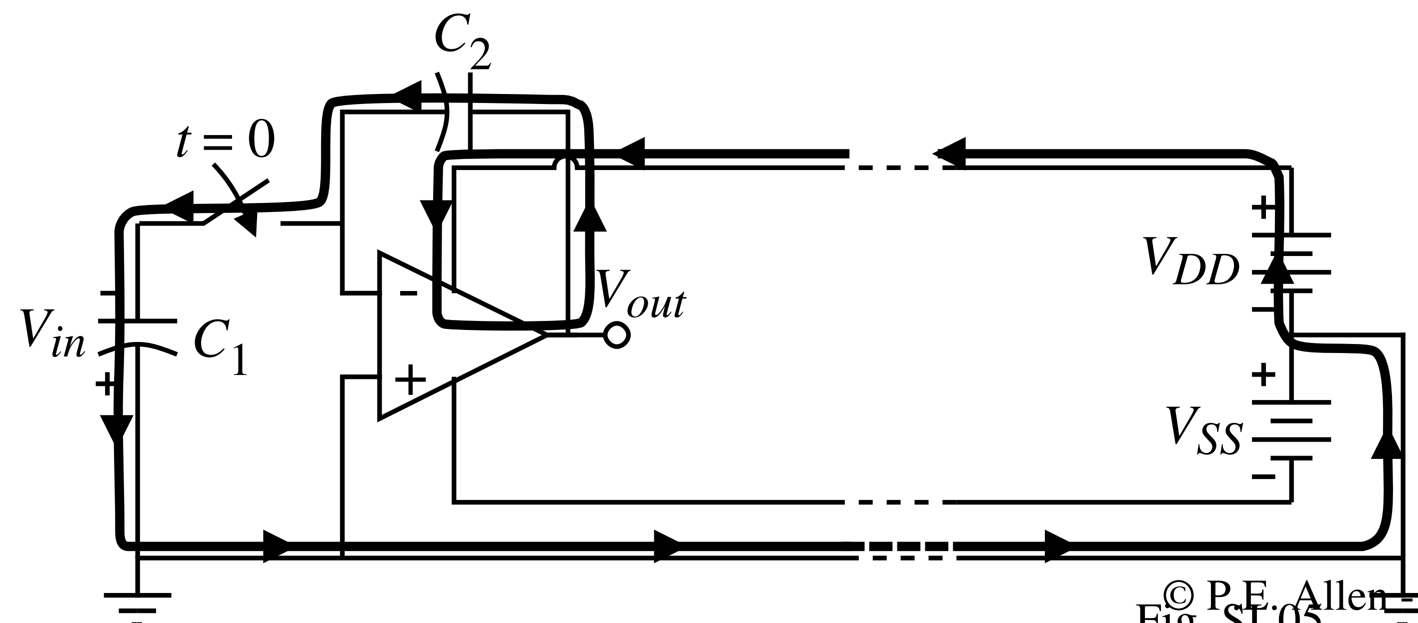

Fig. SI-05

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Summary of Substrate Interference

- Methods to reduce substrate noise
  1.) Physical separation
  2.) Guard rings placed close to the sensitive circuits with dedicated package pins.
  3.) Reduce the inductance in power supply and ground leads (best method)
  4.) Connect regions of constant potential (wells and substrate) to metal with as many contacts as possible.
- Noise Insensitive Circuit Design Techniques
  1.) Design for a high power supply rejection ratio (PSRR)
  2.) Use multiple devices spatially distinct and average the signal and noise.
  3.) Use “quiet” digital logic (power supply current remains constant)
  4.) Use differential signal processing techniques.
- Some references

1.) D.K. Su, M.J. Loinaz, S. Masui and B.A. Wooley, “Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal IC’s,” *J. of Solid-State Circuits*, vol. 28, No. 4, April 1993, pp. 420-430.

2.) K.M. Fukuda, T. Anbo, T. Tsukada, T. Matsuura and M. Hotta, “Voltage-Comparator-Based Measurement of Equivalently Sampled Substrate Noise Waveforms in Mixed-Signal ICs,” *J. of Solid-State Circuits*, vol. 31, No. 5, May 1996, pp. 726-731.

3.) X. Aragones, J. Gonzalez and A. Rubio, *Analysis and Solutions for Switching Noise Coupling in Mixed-Signal ICs*, Kluwer Acadmic Publishers, Boston, MA, 1999.

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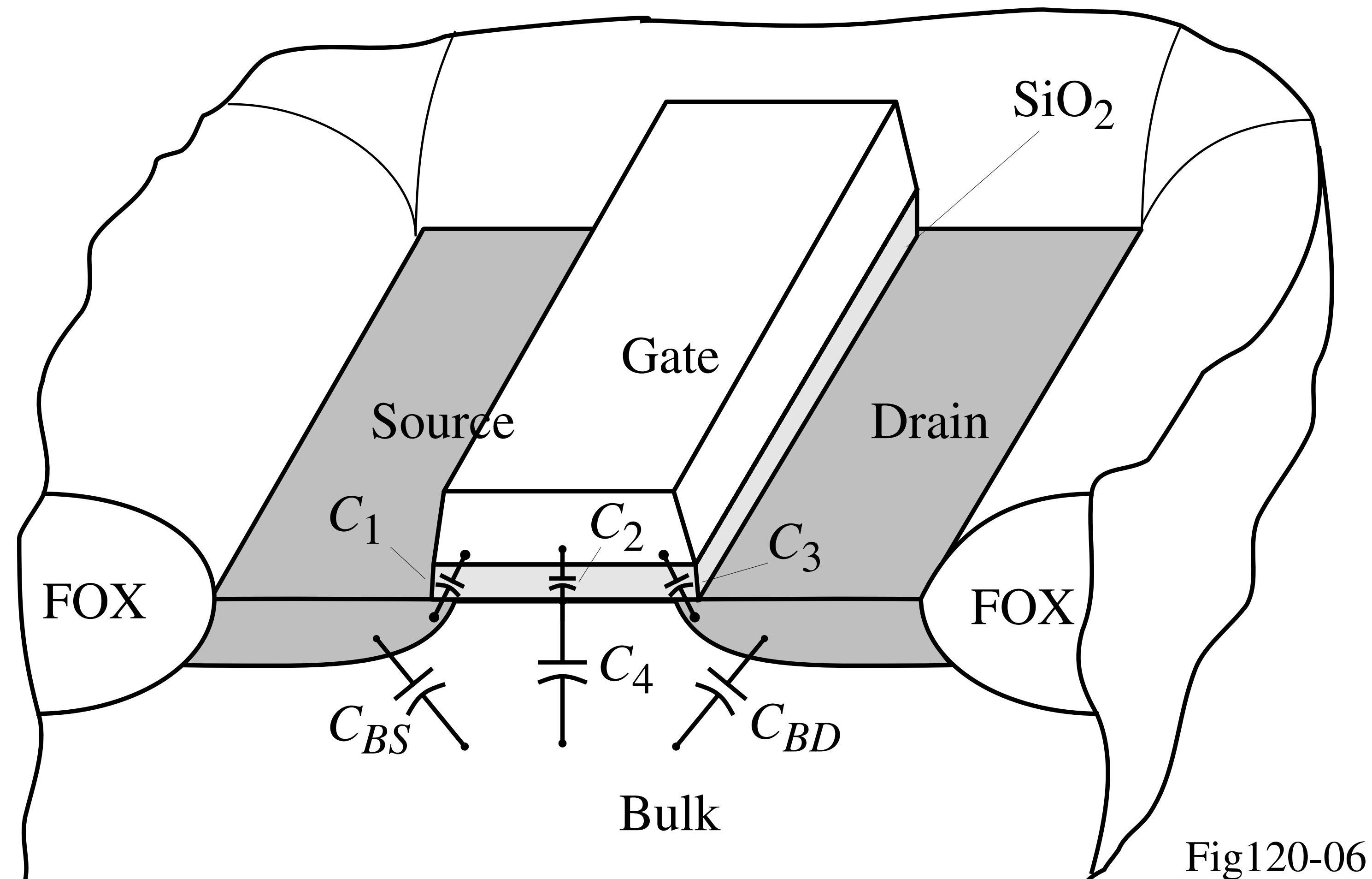
3.4 - CAPACITANCES OF THE MOSFET

Types of Capacitance

Physical Picture:



MOSFET capacitors consist of:

- Depletion capacitances
- Charge storage or parallel plate capacitances

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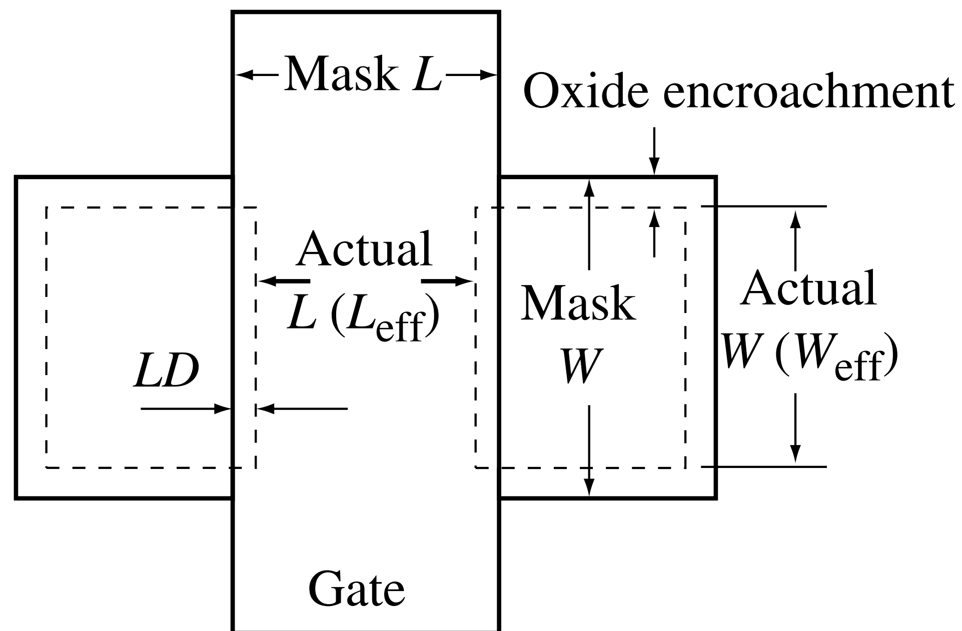
Charge Storage (Parallel Plate) MOSFET Capacitances - C_1, C_2, C_3 and C_4



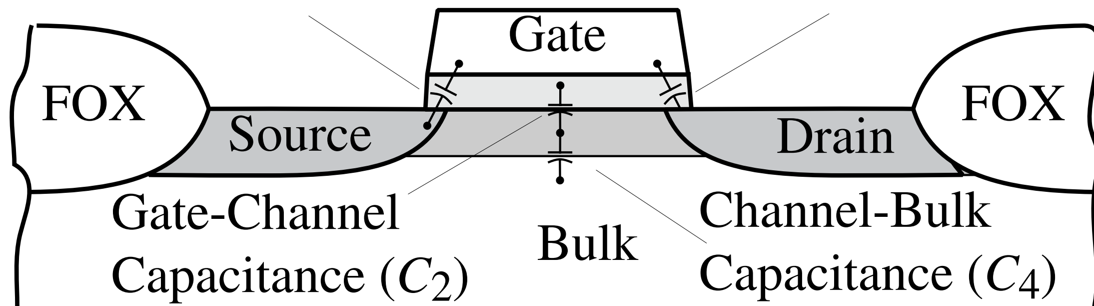


Fig. 120-09

Overlap capacitances:

$C_1 = C_3 = \text{LD}\cdot W_{\text{eff}}\cdot C_{ox}$ = CGSO or CGDO

(LD ≈ 0.015 μm for LDD structures)

Channel capacitances:

C_2 = gate-to-channel = $C_{ox}W_{\text{eff}}\cdot(L\text{-2LD}) = C_{ox}W_{\text{eff}}\cdot L_{\text{eff}}$

C_4 = voltage dependent channel-bulk/substrate capacitance

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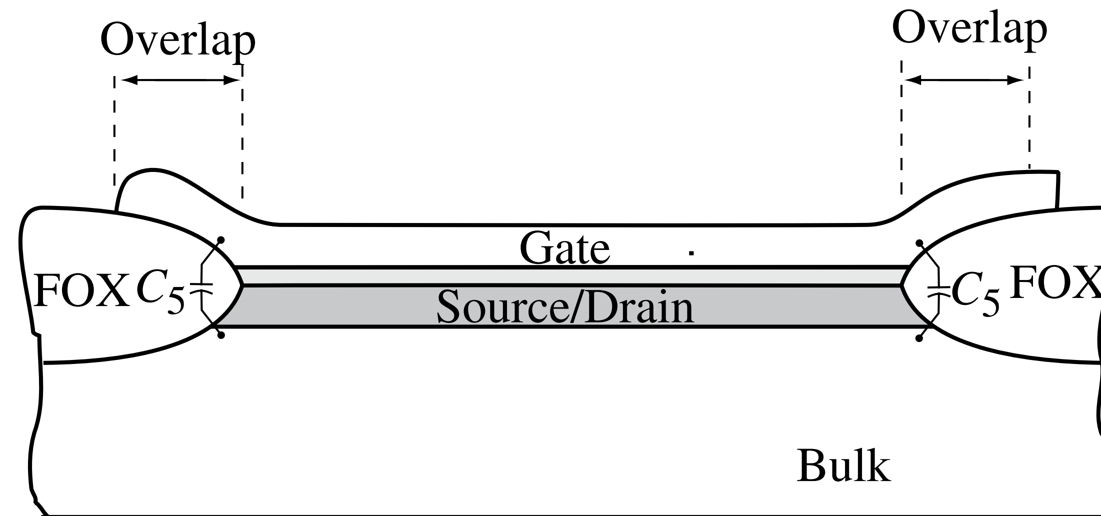
Charge Storage (Parallel Plate) MOSFET Capacitances - C_5

View looking down the channel from source to drain



C_5 = CGBO

Capacitance values based on an oxide thickness of 140 Å or C_{ox}=24.7 × 10^{-4} F/m^2:

Type	P-Channel	N-Channel	Units
CGSO	220×10^{-12}	220×10^{-12}	F/m
CGDO	220×10^{-12}	220×10^{-12}	F/m
CGBO	700×10^{-12}	700×10^{-12}	F/m
CJ	560×10^{-6}	770×10^{-6}	F/m^2
CJSW	350×10^{-12}	380×10^{-12}	F/m
MJ	0.5	0.5	
MJSW	0.35	0.38	

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Illustration of C_{GD}, C_{GS} and C_{GB}

Comments on the variation of C_{BG} in the cutoff region:

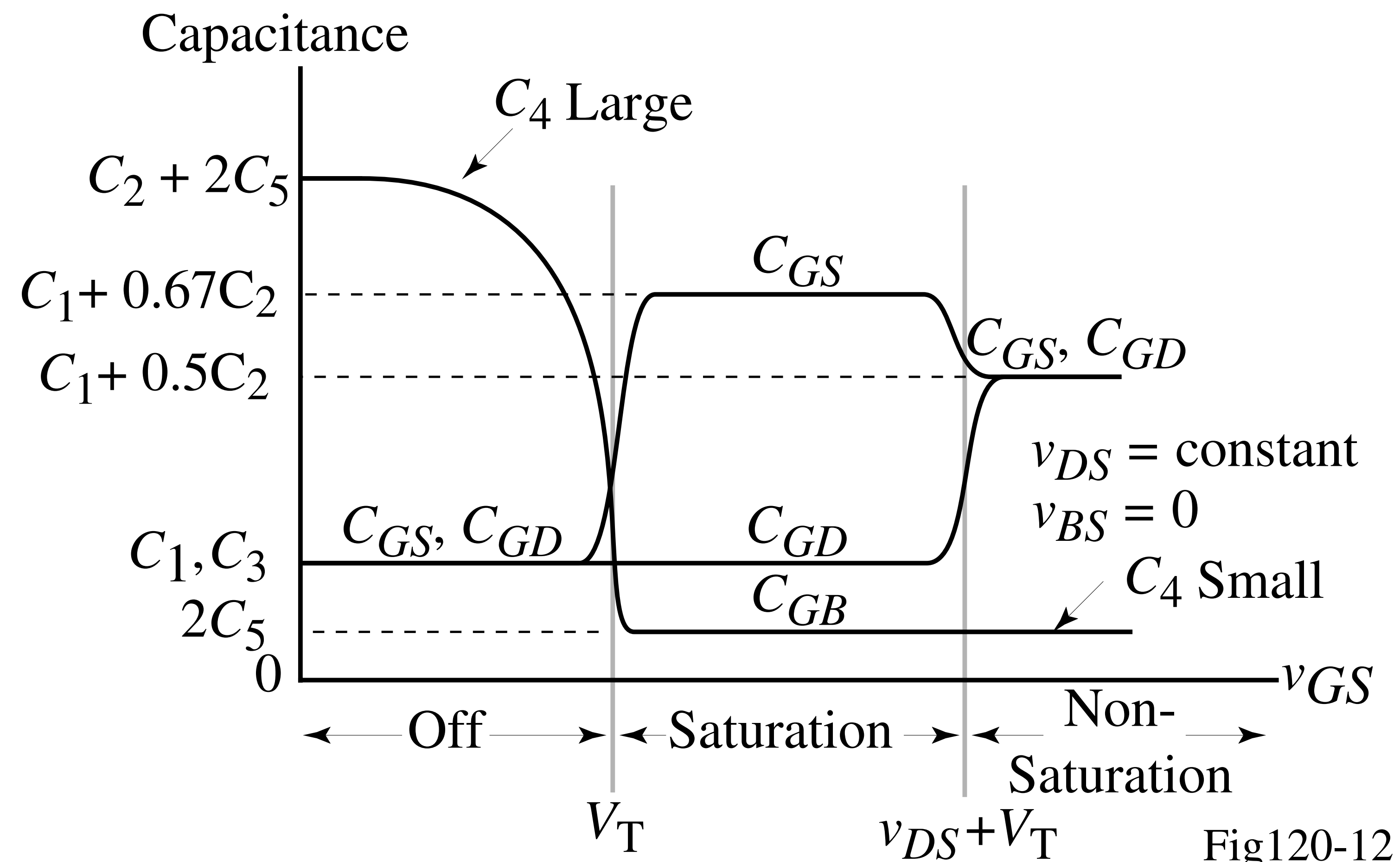
$$C_{BG} = \frac{1}{\frac{1}{C_2} + \frac{1}{C_4}} + 2C_5$$

1.) For $v_{GS} \approx 0$, $C_{GB} \approx C_2 + 2C_5$

(C_4 is large because of the thin inversion layer in weak inversion where V_{GS} is slightly less than V_T))

2.) For $0 < v_{GS} \leq V_T$, $C_{GB} \approx 2C_5$

(C_4 is small because of the thicker inversion layer in strong inversion)



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3.6 - TEMPERATURE AND NOISE MODELS FOR THE MOSFET

Large Signal Temperature Model

Transconductance parameter:

$K'(T) = K'(T_0)\ (T/T_0)^{-1.5}$ (Exponent becomes +1.5 below 77°K)

Threshold Voltage:

$V_T(T) = V_T(T_0) + \alpha(T-T_0) + \cdots$

Typically α_{NMOS} = -2mV/°C to –3mV/°C from 200°K to 400°K (PMOS has a + sign)

Example

Find the value of I_D for a NMOS transistor at 27°C and 100°C if V_{GS} = 2V and W/L = 5µm/1µm if $K'(T_0)$ = 110µA/V² and $V_T(T_0)$ = 0.7V and T_0 = 27°C and α_{NMOS} = -2mV/°C.

Solution

At room temperature, the value of drain current is,

$$I_D(27°C) = \frac{110\mu A/V^2 \cdot 5\mu m}{2\cdot 1\mu m}(2-0.7)^2 = 465\mu A$$

At T = 100°C (373°K), $K'(100°C)=K'(27°C)\ (373/300)^{-1.5}=110\mu A/V^2\cdot 0.72=79.3\mu A/V^2$

and $V_T(100°C) = 0.7 - (.002)(73°C) = 0.554V$

$$\therefore \quad I_D(100°C) = \frac{79.3\mu A/V^2\cdot 5\mu m}{2\cdot 1\mu m}(2-0.554)^2 = 415\mu A$$

(Repeat with V_{GS} = 1.5V)

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Experimental Verification of the MOSFET Temperature Dependence

NMOS Threshold:

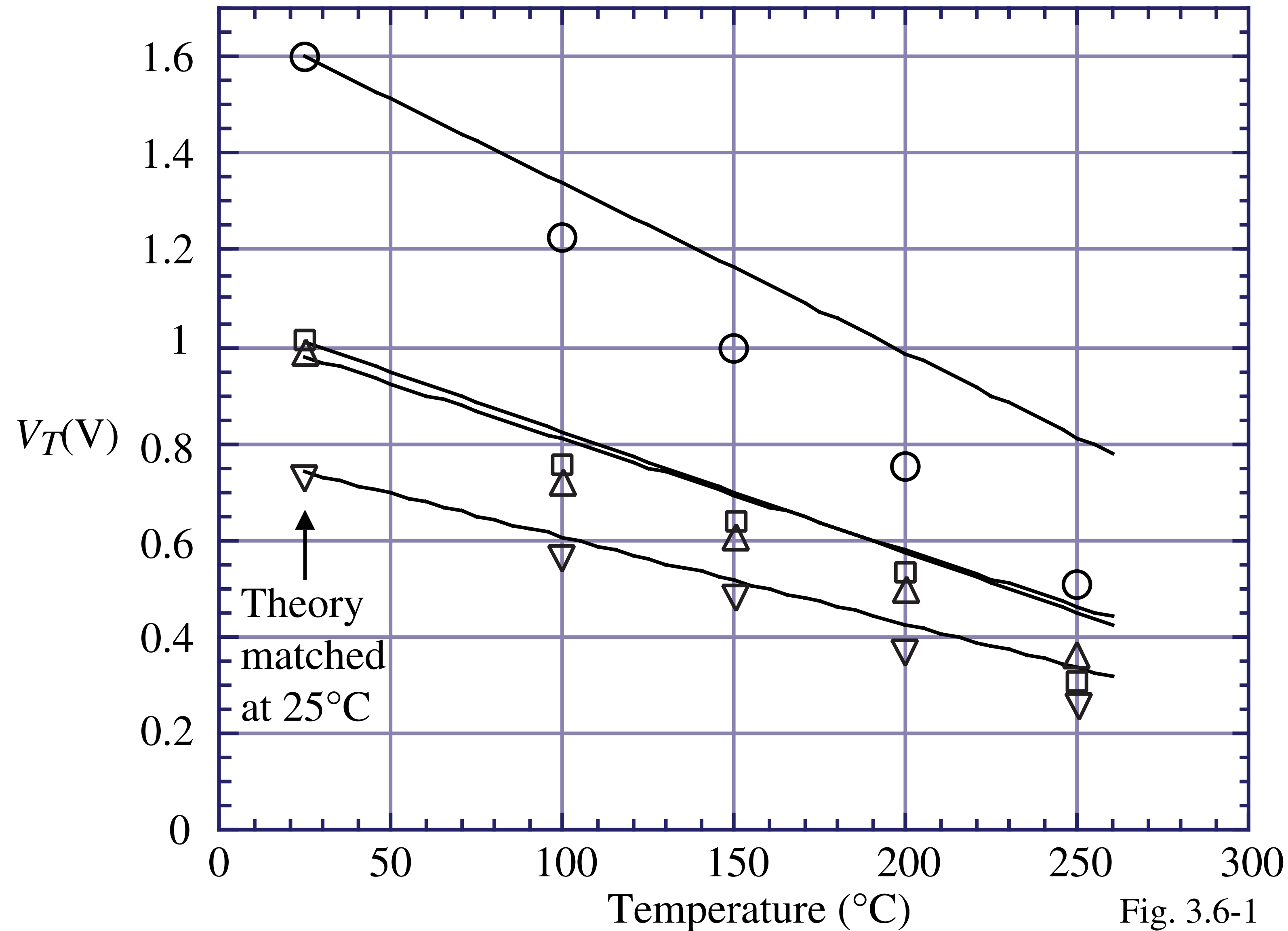

Fig. 3.6-1

Symbol	Min. L	NA (cm-3)	tox (Å)	α (mV/°C)
O	6μm	2x1016	1000	-3.5
❏	5μm	1x1016	650	-2.5
Δ	4μm	2x1016	500	-2.3
∇	2μm	3.3x1016	275	-1.8

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Experimental Verification of the MOSFET Temperature Dependence

PMOS Threshold:

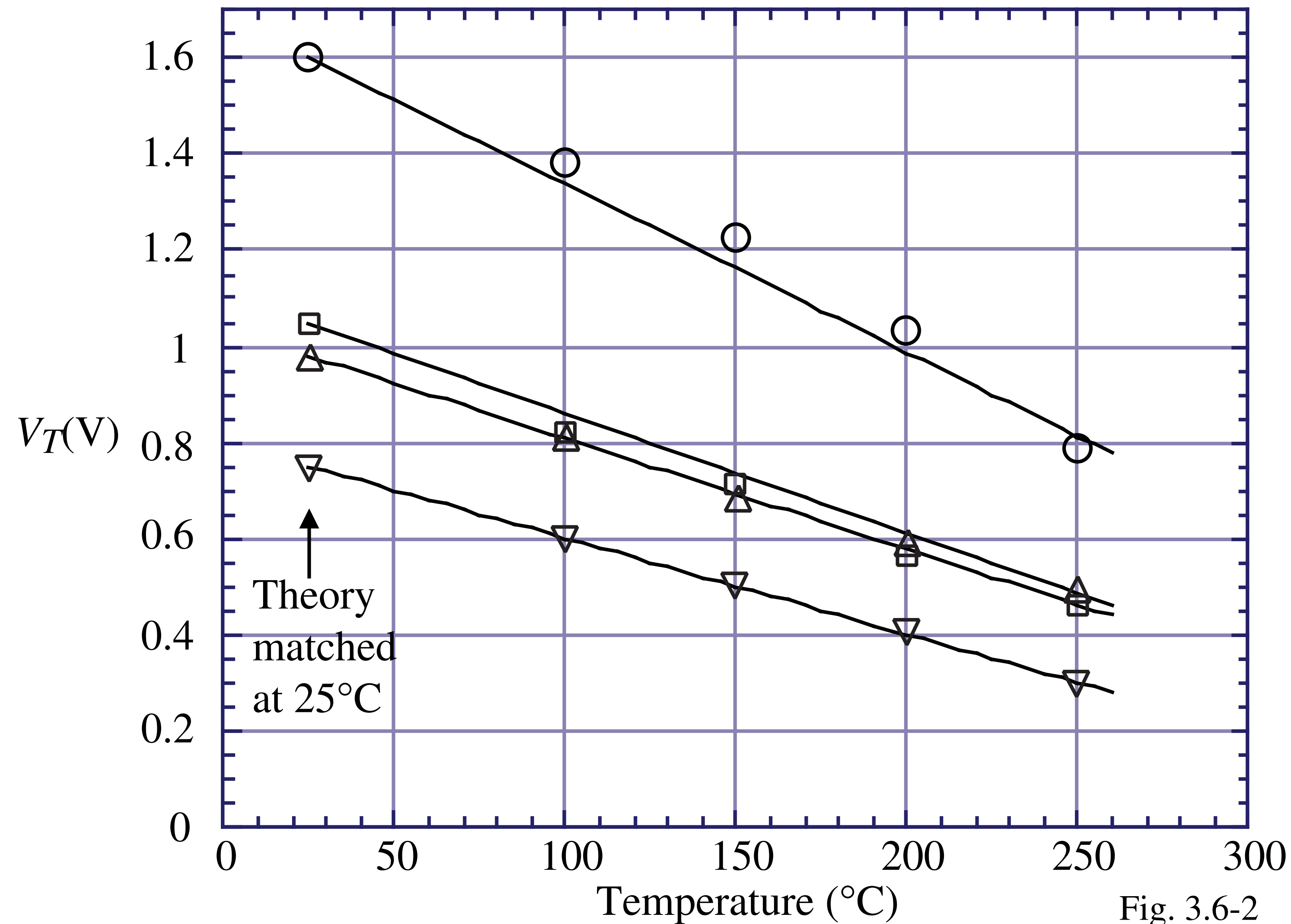

Fig. 3.6-2

Symbol	Min. L	N_A (cm^{-3})	Tox (Å)	α (mV/°C)
O	6µm	2×10^{15}	1000	+3.5
❏	5µm	2×10^{15}	650	+2.5
Δ	4µm	2×10^{16}	500	+2.3
∇	2µm	1.1×10^{16}	275	+2.0

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Zero Temperature Coefficient (ZTC) Point for MOSFETs

For a given value of gate-source voltage, the drain current of the MOSFET will be independent of temperature. Consider the following circuit:

Assume that the transistor is saturated and that:

$$\mu = \mu_o\left(\frac{T}{T_o}\right)^{-1.5} \quad \text{and} \quad V_T(T) = V_T(T_o) + \alpha(T-T_o)$$

where $\alpha = -0.0023\text{V/°C}$ and $T_o = 27\text{°C}$

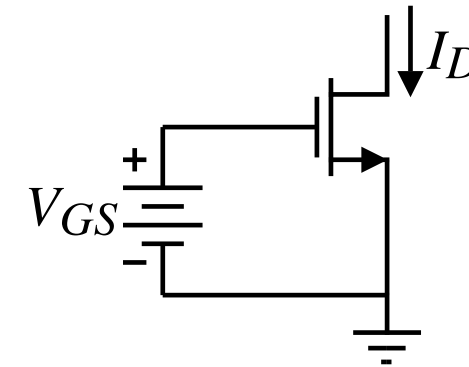

Fig. 4.5-12

$$\therefore \quad I_D(T) = \frac{\mu_o C_{ox} W}{2L}\left(\frac{T}{T_o}\right)^{-1.5}[V_{GS} - V_{T0} - \alpha(T-T_o)]^2$$

$$\frac{dI_D}{dT} = \frac{-1.5\mu_o C_{ox}}{2T_o}\left(\frac{T}{T_o}\right)^{-2.5}[V_{GS}-V_{T0}-\alpha(T-T_o)]^2 + \alpha\mu_o C_{ox}\left(\frac{T}{T_o}\right)^{-1.5}[V_{GS}-V_{T0}-\alpha(T-T_o)] = 0$$

$$\therefore \quad V_{GS} - V_{T0} - \alpha(T-T_o) = \frac{-4T\alpha}{3} \quad \Rightarrow \quad \boxed{V_{GS}(\text{ZTC}) = V_{T0} - \alpha T_o - \frac{\alpha T}{3}}$$

Let $K' = 10\mu\text{A/V}^2$, $W/L = 5$ and $V_{T0} = 0.71\text{V}$.

At T=27°C (300°K), V_{GS}(ZTC)=0.71-(-0.0023)(300°K)-(0.333)(-0.0023)(300°K) = 1.63V

At T = 27°C (300°K), $I_D = (10\mu\text{A/V}^2)(5/2)(1.63-0.71)^2 = 21.2\mu\text{A}$

At T=200°C (473°K), V_{GS}(ZTC)=0.71-(-0.0023)(300°K)-(0.333)(-0.0023)(473°K)=1.76V

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Experimental Verification of the ZTC Point

The data below is for a 5μm n-channel MOSFET with W/L=50μm/10μm, N_A=10^{16} cm^{-3}, t_{ox} = 650Å, u_oC_{ox} = 10μA/V^2, and V_{T0} = 0.71V.

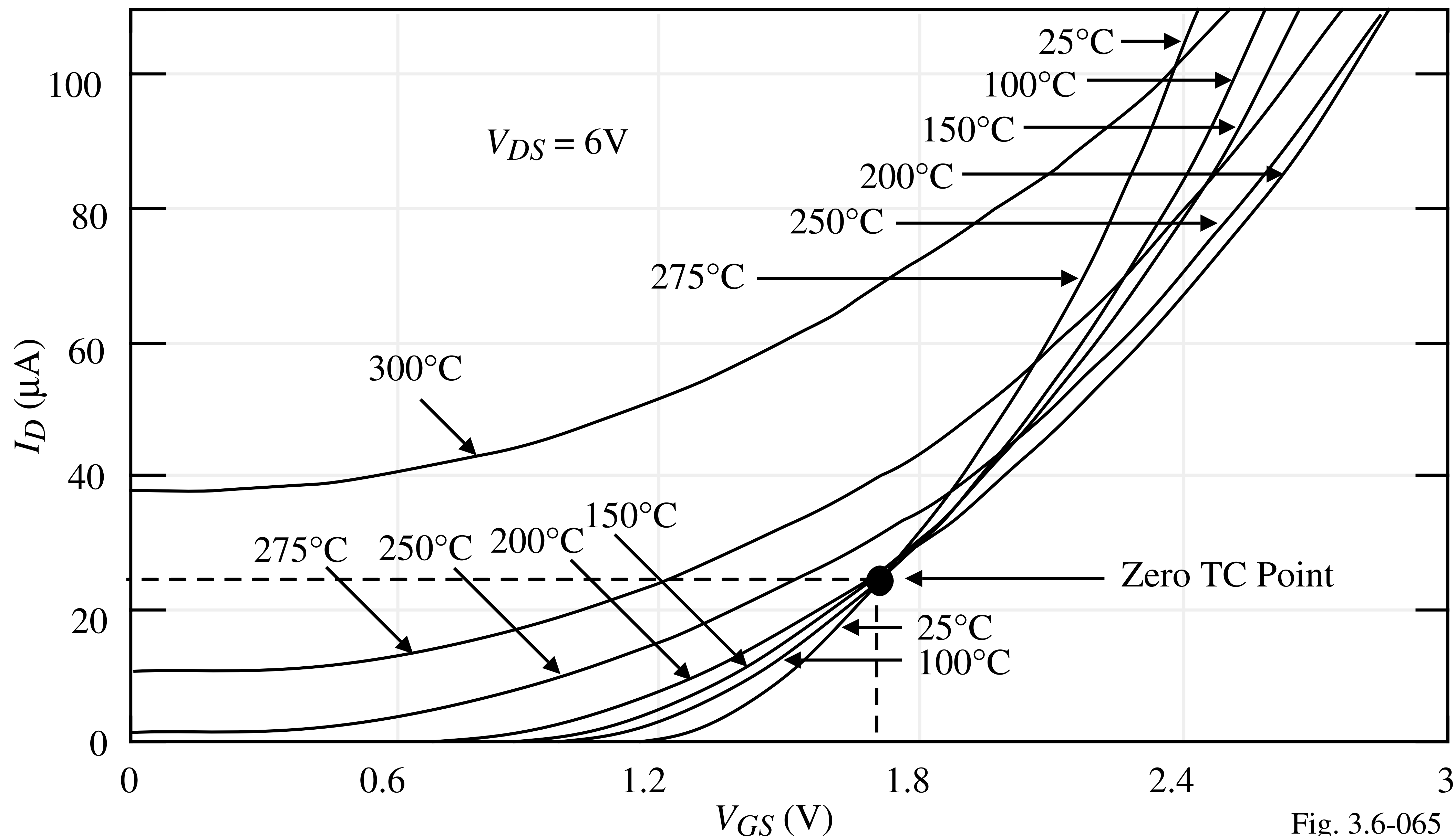


Fig. 3.6-065

ZTC Point for PMOS

The data is for a 5μm p-channel MOSFET with W/L=50μm/10μm, N_D=2x10^{-15}cm^{-3}, and t_{ox} = 650Å.

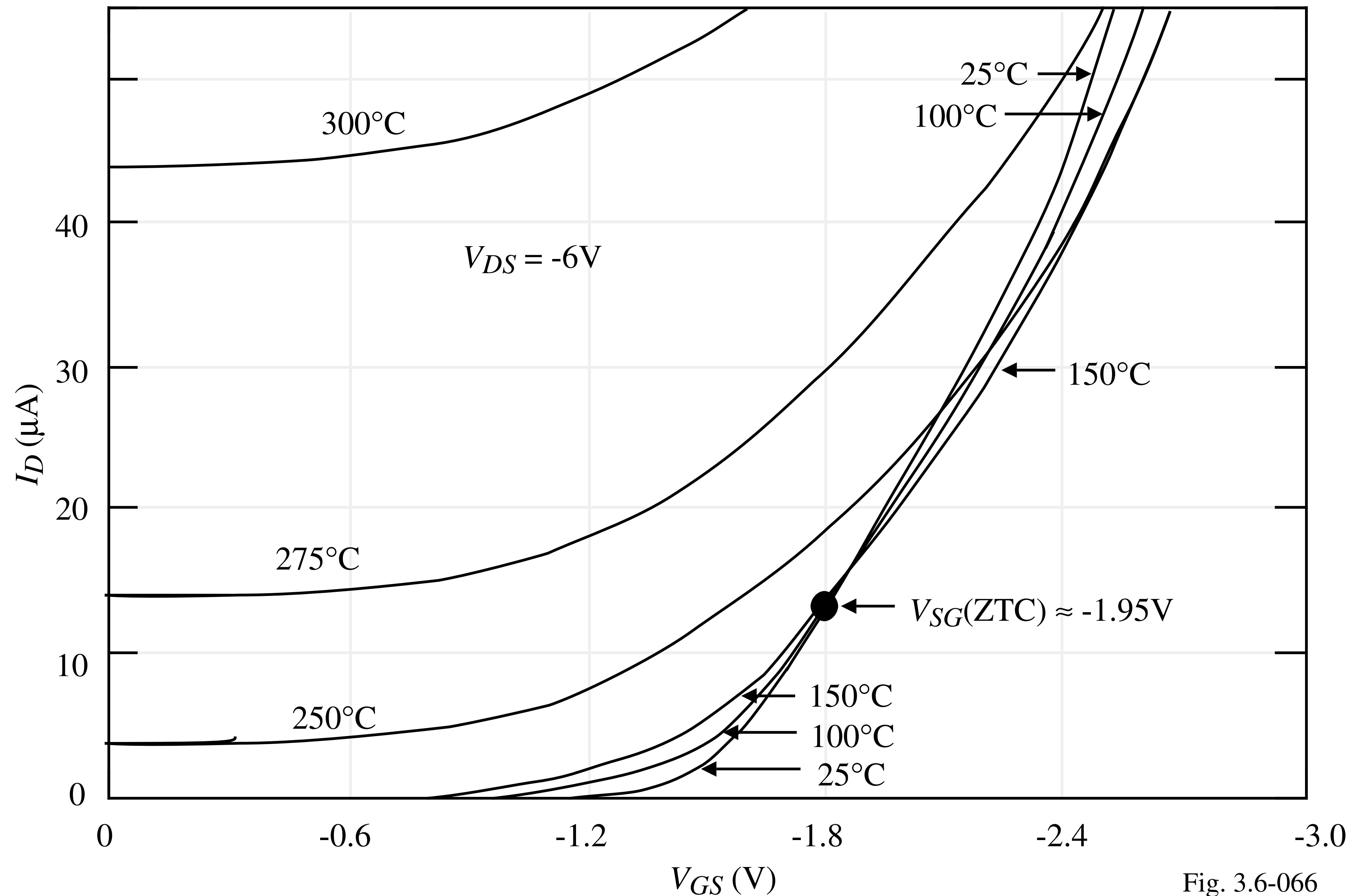
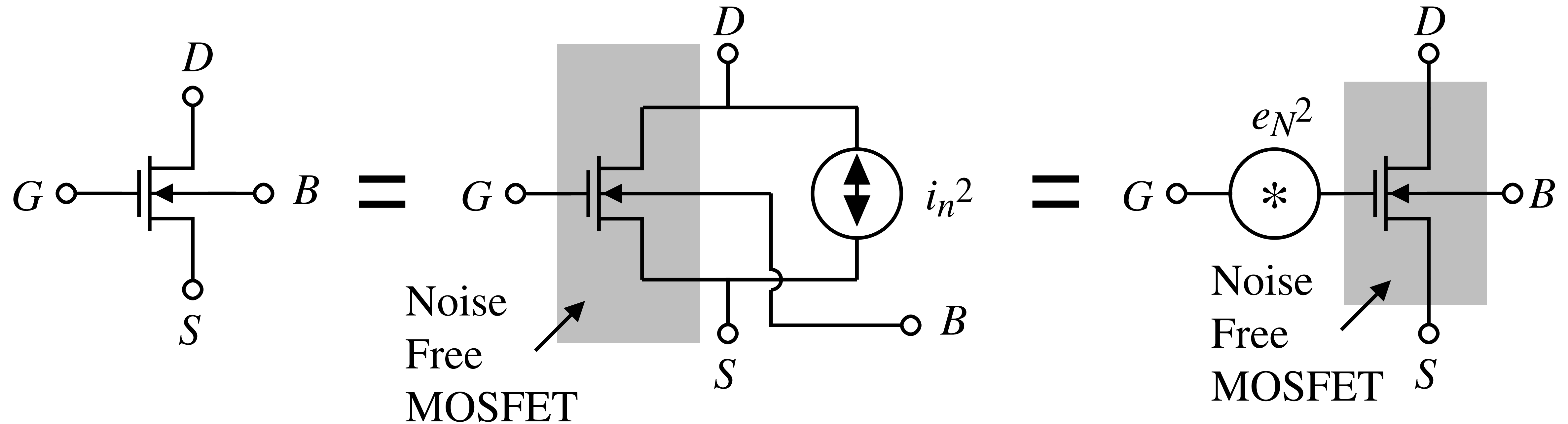


Fig. 3.6-066

Zero temperature coefficient will occur for every MOSFET up to about 200°C.

MOSFET NOISE

MOS Device Noise at Low Frequencies



where

$$i_n^2 = \left[\frac{8kTg_m(1+\eta)}{3} + \frac{KF\, I_D}{f^S C_{ox} L^2}\right]\Delta f \quad \text{(amperes}^2\text{)}$$

Δf = bandwidth at a frequency, f

$$\eta = \frac{g_{mbs}}{g_m}$$

k = Boltzmann’s constant

KF = Flicker noise coefficient

S = Slope factor of the 1/f noise

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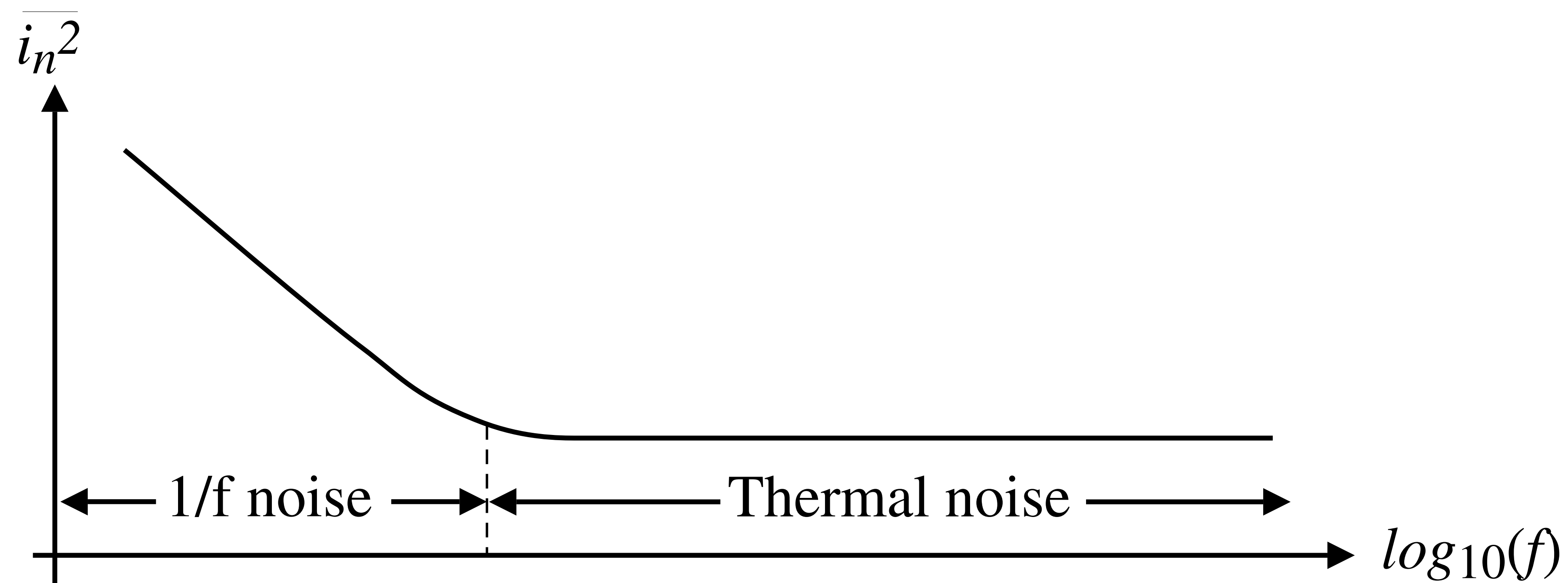
Reflecting the MOSFET Noise to the Gate

Dividing i_n^2 by g_m^2 gives

$$e_n^2 = \frac{i_n^2}{g_m^2} = \left[\frac{8kT(1+\eta)}{3g_m} + \frac{KF}{2fC_{ox}WL\,K'} \right] \Delta f \quad \text{(volts}^2\text{)}$$

It will be convenient to use $B = \dfrac{KF}{2C_{ox}K'}$ for model simplification.



SEC. 3.9 – MODELS FOR SIMULATION OF MOS CIRCUITS

FET Model Generations

- First Generation – Physically based analytical model including all geometry dependence.
- Second Generation – Model equations became subject to mathematical conditioning for circuit simulation. Use of empirical relationships and parameter extraction.
- Third Generation – A return to simpler model structure with reduced number of parameters which are physically based rather than empirical. Uses better methods of mathematical conditioning for simulation including more specialized smoothing functions.

Performance Comparison of Models (from Cheng and Hu, *MOSFET Modeling & BSIM3 Users Guide*)

Model	Minimum L (μm)	Minimum Tox (nm)	Model Continuity	i_D Accuracy in Strong Inversion	i_D Accuracy in Subthreshold	Small signal parameter	Scalability
MOS1	5	50	Poor	Poor	Not Modeled	Poor	Poor
MOS2	2	25	Poor	Poor	Poor	Poor	Fair
MOS3	1	20	Poor	Fair	Poor	Poor	Poor
BSIM1	0.8	15	Fair	Good	Fair	Poor	Fair
BSIM2	0.35	7.5	Fair	Good	Good	Fair	Fair
BSIM3v2	0.25	5	Fair	Good	Good	Good	Good
BSIM3v3	0.15	4	Good	Good	Good	Good	Good

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First Generation Models

Level 1 (MOS1)

- Basic square law model based on the gradual channel approximation and the square law for saturated drain current.
- Good for hand analysis.
- Needs improvement for deep-submicron technology (must incorporate the square law to linear shift)

Level 2 (MOS2)

- First attempt to include small geometry effects
- Inclusion of the channel-bulk depletion charge results in the familiar 3/2 power terms
- Introduced a simple subthreshold model which was not continuous with the strong inversion model.
- Model became quite complicated and probably is best known as a “developing ground” for better modeling techniques.

Level 3 (MOS3)

- Used to overcome the limitations of Level 2. Made use of a semi-empirical approach.
- Added DIBL and the reduction of mobility by the lateral field.
- Similar to Level 2 but considerably more efficient.
- Used binning but was poorly implemented.

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Second Generation Models

BSIM (Berkeley Short-Channel IGFET Model)

- Emphasis is on mathematical conditioning for circuit simulation
- Short channel models are mostly empirical and shifts the modeling to the parameter extraction capability
- Introduced a more detailed subthreshold current model with good continuity
- Poor modeling of channel conductance

HSPICE Level 28

- Based on BSIM but has been extensively modified.
- More suitable for analog circuit design
- Uses model binning
- Model parameter set is almost entirely empirical
- User is locked into HSPICE
- Model is proprietary

BSIM2

- Closely based on BSIM
- Employs several expressions developed from two dimensional analysis
- Makes extensive modifications to the BSIM model for mobility and the drain current
- Uses a new subthreshold model
- Output conductance model makes the model very suitable for analog circuit design
- The drain current model is more accurate and provides better convergence
- Becomes more complex with a large number of parameters
- No provisions for variations in the operating temperature

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Third Generation Models

BSIM3

- This model has achieved stability and is being widely used in industry for deep submicron technology.
- Initial focus of simplicity was not realized.

MOS Model 9

- Developed at Philips Laboratory
- Has extensive heritage of industrial use
- Model equations are clean and simple – should be efficient

Other Candidates

- EKV (Enz-Krummenacher-Vittoz) – fresh approach well suited to the needs of analog circuit design

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BSIM2 Model used in Subthreshold

```
BSIM Model Parameters used in Subthreshold
VDS 1 0 DC 3.0
M1 1 1 0 0 CMOSN W=5UM L=2UM
.MODEL CMOSN NMOS LEVEL=4
+VFB=-7.92628E-01     LVFB= 1.22972E-02     WVFB=-1.00233E-01
+PHI= 7.59099E-01     LPHI= 0.00000E+00     WPHI= 0.00000E+00
+K1= 1.06705E+00      LK1= 5.08430E-02      WK1= 4.72787E-01
+K2=-4.23365E-03      LK2= 6.76974E-02      WK2= 6.27415E-02
+ETA=-4.30579E-03     LETA= 9.05179E-03     WETA= 7.33154E-03
+MUZ= 5.58459E+02     DL=6.86137E-001       DW=-1.04701E-001
+U0= 5.52698E-02      LU0= 6.09430E-02      WU0=-6.91423E-02
+U1= 5.38133E-03      LU1= 5.43387E-01      WU1=-8.63357E-02
+X2MZ= 1.45214E+01    LX2MZ=-3.08694E+01    WX2MZ= 4.75033E+01
+X2E=-1.67104E-04     LX2E=-4.75323E-03     WX2E=-2.74841E-03
+X3E= 5.33407E-04     LX3E=-4.69455E-04     WX3E=-5.26199E-03
+X2U0= 2.45645E-03    LX2U0=-1.46188E-02    WX2U0= 2.63555E-02
+X2U1=-3.80979E-04    LX2U1=-1.71488E-03    WX2U1= 2.23520E-02
+MUS= 5.48735E+02     LMUS= 3.28720E+02     WMUS= 1.35360E+02
+X2MS= 6.72261E+00    LX2MS=-3.48094E+01    WX2MS= 9.84809E+01
+X3MS=-2.79427E+00    LX3MS= 6.31555E+01    WX3MS=-1.99720E-01
+X3U1= 1.18671E-03    LX3U1= 6.13936E-02    WX3U1=-3.49351E-03
+TOX=4.03000E-002     TEMP= 2.70000E+01     VDD= 5.00000E+00
+CGDO=4.40942E-010    CGSO=4.40942E-010     CGBO=6.34142E-010
+XPART=-1.00000E+000
+N0=1.00000E+000      LN0=0.00000E+000      WN0=0.00000E+000
+NB=0.00000E+000      LNB=0.00000E+000      WNB=0.00000E+000
+ND=0.00000E+000      LND=0.00000E+000      WND=0.00000E+000
+RSH=0 CJ=4.141500e-04  CJSW=4.617400e-10   JS=0   PB=0.8
+PBSW=0.8    MJ=0.4726    MJSW=0.3597    WDF=0   DELL=0
.DC VDS 5.0 0 0.01
.PRINT DC ID(M1)
.PROBE
.END
```

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BSIM3 Model

The background for the BSIM3 model and the equations are given in detail in the text *MOSFET Modeling & BSIM3 User's Guide*, by Y. Cheng and C. Hu, Kluwer Academic Publishers, 1999.

The short channel effects included in the BSIM3 model are:

- Normal and reverse short-channel and narrow-width effects on the threshold.
- Channel length modulation (*CLM*).
- Drain induced barrier lowering (*DIBL*).
- Velocity saturation.
- Mobility degradation due to the vertical electric field.
- Impact ionization.
- Band-to-band tunnelling.
- Velocity overshoot.
- Self-heating.

1.) Channel quantiztion.

2.) Polysilicon depletion.

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0.25µm BSIM3v3.1 NMOS Parameters

```
.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1          TNOM    = 27            TOX     = 5.7E-9
+XJ      = 1E-7         NCH     = 2.3549E17     VTH0    = 0.4273342
+K1      = 0.3922983    K2      = 0.0185825     K3      = 1E-3
+K3B     = 2.0947677    W0      = 2.171779E-7   NLX     = 1.919758E-7
+DVT0W   = 0            DVT1W   = 0             DVT2W   = 0
+DVT0    = 7.137212E-3  DVT1    = 6.066487E-3   DVT2    = -0.3025397
+U0      = 403.1776038  UA      = -3.60743E-12  UB      = 1.323051E-18
+UC      = 2.575123E-11 VSAT    = 1.616298E5    A0      = 1.4626549
+AGS     = 0.3136349    B0      = 3.080869E-8   B1      = -1E-7
+KETA    = 5.462411E-3  A1      = 4.653219E-4   A2      = 0.6191129
+RDSW    = 345.624986   PRWG    = 0.3183394     PRWB    = -0.1441065
+WR      = 1            WINT    = 8.107812E-9   LINT    = 3.375523E-9
+XL      = 3E-8         XW      = 0             DWG     = 6.420502E-10
+DWB     = 1.042094E-8  VOFF    = -0.1083577    NFACTOR = 1.1884386
+CIT     = 0            CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0            ETA0    = 4.914545E-3   ETAB    = 4.215338E-4
+DSUB    = 0.0313287    PCLM    = 1.2088426     PDIBLC1 = 0.7240447
+PDIBLC2 = 5.120303E-3  PDIBLCB = -0.0443076    DROUT   = 0.7752992
+PSCBE1  = 4.451333E8   PSCBE2  = 5E-10         PVAG    = 0.2068286
+DELTA   = 0.01         MOBMOD  = 1             PRT     = 0
+UTE     = -1.5         KT1     = -0.11         KT1L    = 0
+KT2     = 0.022        UA1     = 4.31E-9       UB1     = -7.61E-18
+UC1     = -5.6E-11     AT      = 3.3E4         WL      = 0
+WLN     = 1            WW      = -1.22182E-16  WWN     = 1.2127
+WWL     = 0            LL      = 0             LLN     = 1
+LW      = 0            LWN     = 1             LWL     = 0
+CAPMOD  = 2            XPART   = 0.4           CGDO    = 6.33E-10
+CGSO    = 6.33E-10     CGBO    = 1E-11         CJ      = 1.766171E-3
+PB      = 0.9577677    MJ      = 0.4579102     CJSW    = 3.931544E-10
+PBSW    = 0.99         MJSW    = 0.2722644     CF      = 0
+PVTH0   = -2.126483E-3 PRDSW   = -24.2435379   PK2     = -4.788094E-4
+WKETA   = 1.430792E-3  LKETA   = -6.548592E-3  )
```

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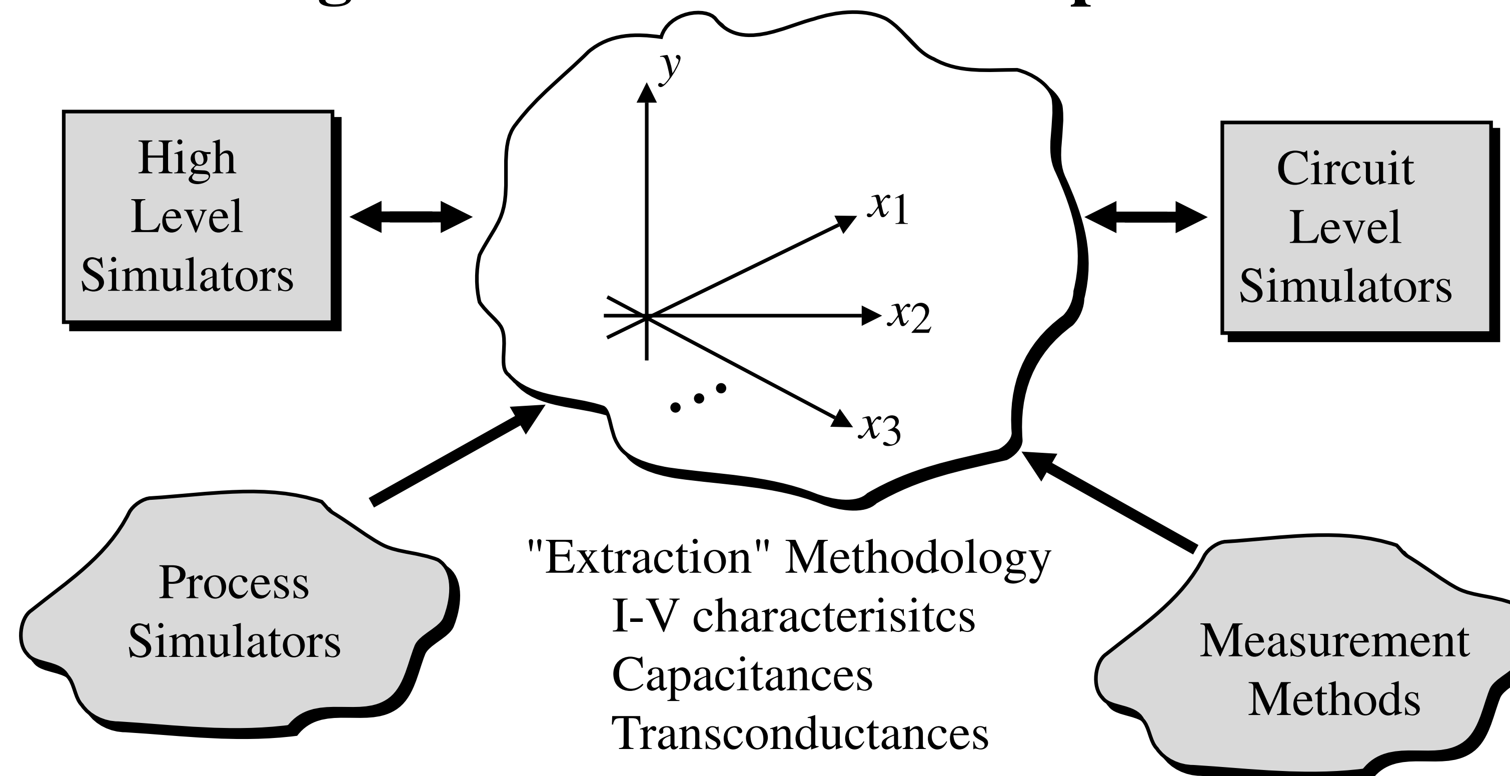
Adjustable Precision Analog Models – Table Lookup



- Objective

  Develop models having adjustable precision in ac and dc perfomrance using table lookup models.

- Advantages

  Usable at any level – device, circuit, or behavioral

  Quickly developed from experiment or process simulators

  Faster than analytical device models (BSIM)

- Disadvantages

  Requires approximately 10kbytes for a typical MOS model

  Can't be parameterized easily

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Summary of MOSFET Models for Simulation

- Models are much improved for efficient computer simulation
- Output conductance model is greatly improved
- Poor results for narrow channel transistors
- Can have discontinuities at bin boundaries
- Fairly complex model, difficult to understand in detail

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SEC. 3.10 – EXTRACTION OF A LARGE SIGNAL MODEL FOR HAND CALCULATIONS

Objective

Extract a simple model that is useful for design from the computer models such as BSIM3.

Extraction for Short Channel Models

Procedure for extracting short channel models:

1.) Extract the square-law model parameters for a transistor with length at least 10 times L_{min}.

2.) Using the values of K', V_T, λ, and γ extract the model parameters for the following model:

$$i_D = \frac{K'}{2[1+\theta(v_{GS}-V_T)]}\frac{W}{L}[v_{GS}-V_T]^2(1+\lambda v_{DS})$$

Adjust the values of K', V_T, and λ as needed.

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EXTRACTION OF THE SIMPLE, SQUARE-LAW MODEL

Characterization of the Simple Square-Law Model

Equations for the MOSFET in strong inversion:

$$i_D = K\left(\frac{W_{\text{eff}}}{2L_{\text{eff}}}\right)(v_{GS} - V_T)^2(1 + \lambda v_{DS}) \quad (1)$$

$$i_D = K\left(\frac{W_{\text{eff}}}{L_{\text{eff}}}\right)\left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right](1 + \lambda v_{DS}) \quad (2)$$

where

$$V_T = V_{T0} + \gamma\left[\sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|}\right] \quad (3)$$

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Extraction of Model Parameters:

First assume that v_{DS} is chosen such that the λv_{DS} term in Eq. (2) is much less than one and v_{SB} is zero, so that $V_T = V_{T0}$.

Therefore, Eq. (2) simplifies to

$$i_D = K'\left(\frac{W_{\text{eff}}}{2L_{\text{eff}}}\right)(v_{GS} - V_{T0})^2 \tag{6}$$

This equation can be manipulated algebraically to obtain the following

$$i_D^{1/2} = \left(\frac{K' W_{\text{eff}}}{2L_{\text{eff}}}\right)^{1/2} v_{GS} = \left(\frac{K' W_{\text{eff}}}{2L_{\text{eff}}}\right)^{1/2} V_{T0} \tag{7}$$

which has the form

$$y = mx + b \tag{8}$$

This equation is easily recognized as the equation for a straight line with m as the slope and b as the y-intercept. Comparing Eq. (7) to Eq. (8) gives

$$y = i_{\text{D}}^{1/2} \tag{9}$$

$$x = v_{GS} \tag{10}$$

$$m = \left(\frac{K' W_{\text{eff}}}{2L_{\text{eff}}}\right)^{1/2} \tag{11}$$

and

$$b = -\left(\frac{K' W_{\text{eff}}}{2L_{\text{eff}}}\right)^{1/2} V_{T0} \tag{12}$$

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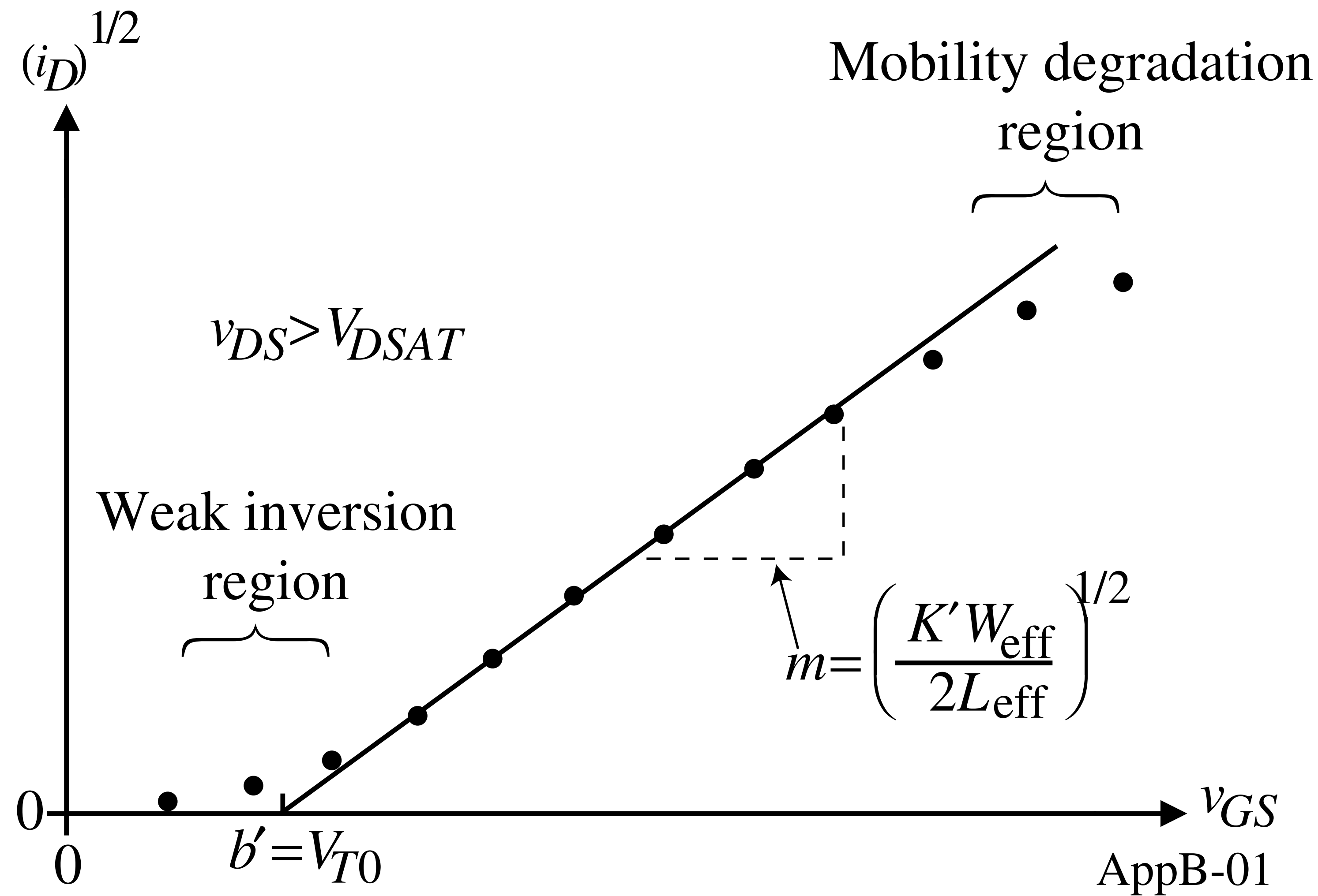
Illustration of *K'* and V_T Extraction



Comments:

- Stay away from the extreme regions of mobility degradation and weak inversion
- Use channel lengths greater than L_{min}

Example 3.10-1 – Extraction of K' and V_T Using Linear Regression

Given the following transistor data shown in Table 3.10-1 and linear regression formulas based on the form,

$$y = mx + b \tag{13}$$

and

$$m = \frac{\sum x_i y_i - (\sum x_i \sum y_i)/n}{\sum x_i^2 - (\sum x_i)^2/n} \tag{14}$$

determine V_{T0} and $K\ W/2L$. The data in Table B-1 also give $I_D^{1/2}$ as a function of V_{GS}.

Table 3.10-1 Data for Example 3.10-1

V_{GS} (V)	I_D (μA)	$\sqrt{I_D}$ (μA)$^{1/2}$	V_{SB} (V)
1.000	0.700	0.837	0.000
1.200	2.00	1.414	0.000
1.500	8.00	2.828	0.000
1.700	13.95	3.735	0.000
1.900	22.1	4.701	0.000

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Example 3.10-1 – Continued

Solution

The data must be checked for linearity before linear regression is applied. Checking slopes between data points is a simple numerical technique for determining linearity. Using the formula that

$$\text{Slope} = m = \frac{\Delta y}{\Delta x} = \frac{\sqrt{I_{D2}} - \sqrt{I_{D1}}}{V_{GS2} - V_{GS1}}$$

Gives

$$m_1 = \frac{1.414 - 0.837}{0.2} = 2.885 \qquad m_2 = \frac{2.828 - 1.414}{0.3} = 4.713$$

$$m_3 = \frac{3.735 - 2.828}{0.2} = 4.535 \qquad m_4 = \frac{4.701 - 3.735}{0.2} = 4.830$$

These results indicate that the first (lowest value of V_{GS}) data point is either bad, or at a point where the transistor is in weak inversion. This data point will not be included in subsequent analysis. Performing the linear regression yields the following results.

$$V_{T0} = 0.898\ \text{V} \qquad \text{and} \qquad \frac{K'W_{\text{eff}}}{2L_{\text{eff}}} = 21.92\ \mu\text{A/V}^2$$

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Extraction of the Bulk-Threshold Parameter γ

Using the same techniques as before, the following equation

$$V_T = V_{T0} + \gamma\,[\sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|}\,]$$

is written in the linear form where

$$y = V_T \tag{18}$$

$$x = \sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|} \tag{19}$$

$$m = \gamma \tag{20}$$

$$b = V_{T0} \tag{21}$$

The term $2|\phi_F|$ is unknown but is normally in the range of 0.6 to 0.7 volts.

Procedure:

1.) Pick a value for $2|\phi_F|$.

2.) Extract a value for γ.

3.) Calculate N_{SUB} using the relationship, $\gamma = \dfrac{\sqrt{2\varepsilon_{si} q N_{SUB}}}{C_{ox}}$

4.) Calculate ϕ_F using the relationship, $\phi_F = -\dfrac{kT}{q}\ln\left(\dfrac{N_{SUB}}{n_i}\right)$

5.) Iterative procedures can be used to achieve the desired accuracy of γ and $2|\phi_F|$. Generally, an approximate value for $2|\phi_F|$ gives adequate results.

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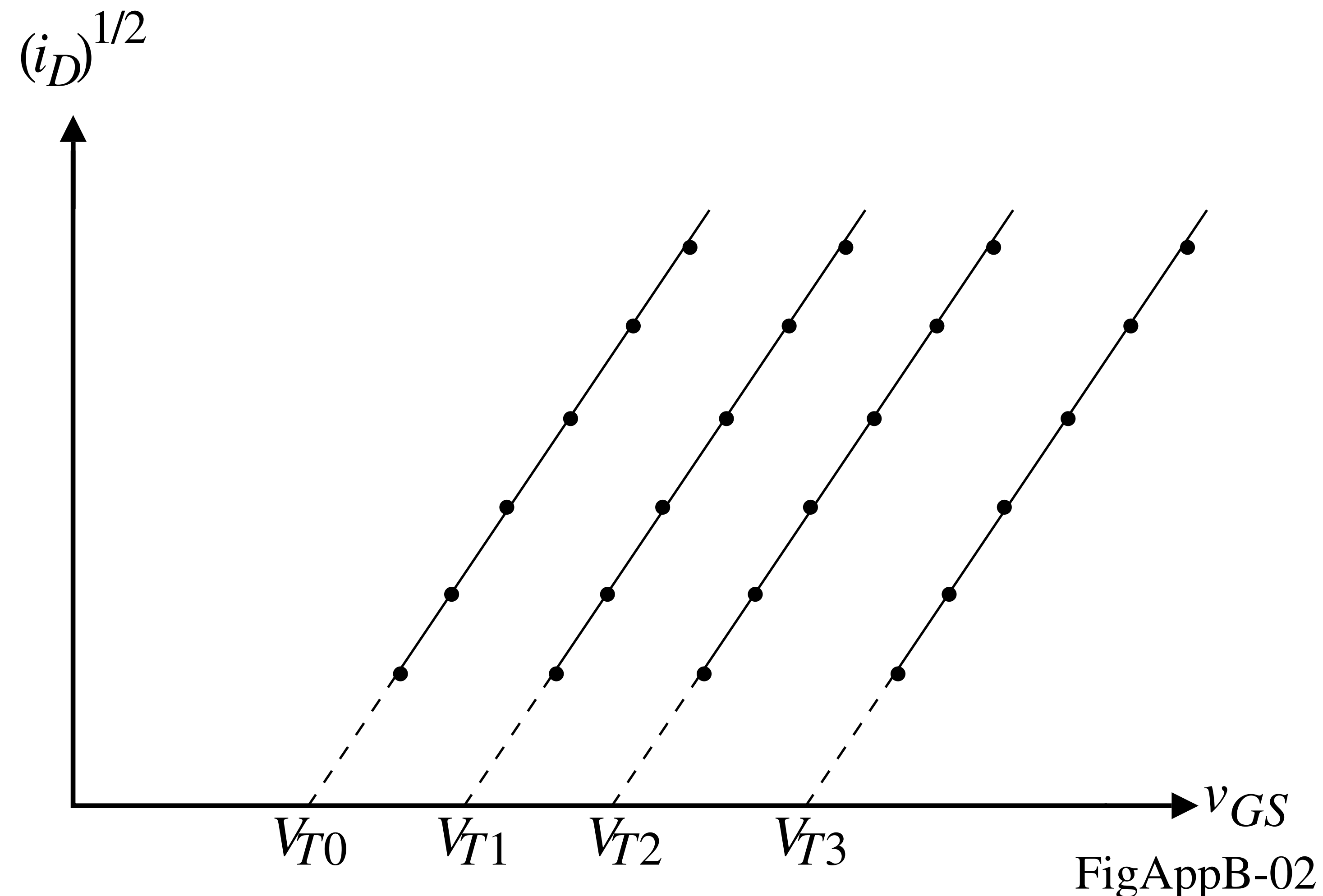
Illustration of the Procedure for Extracting γ

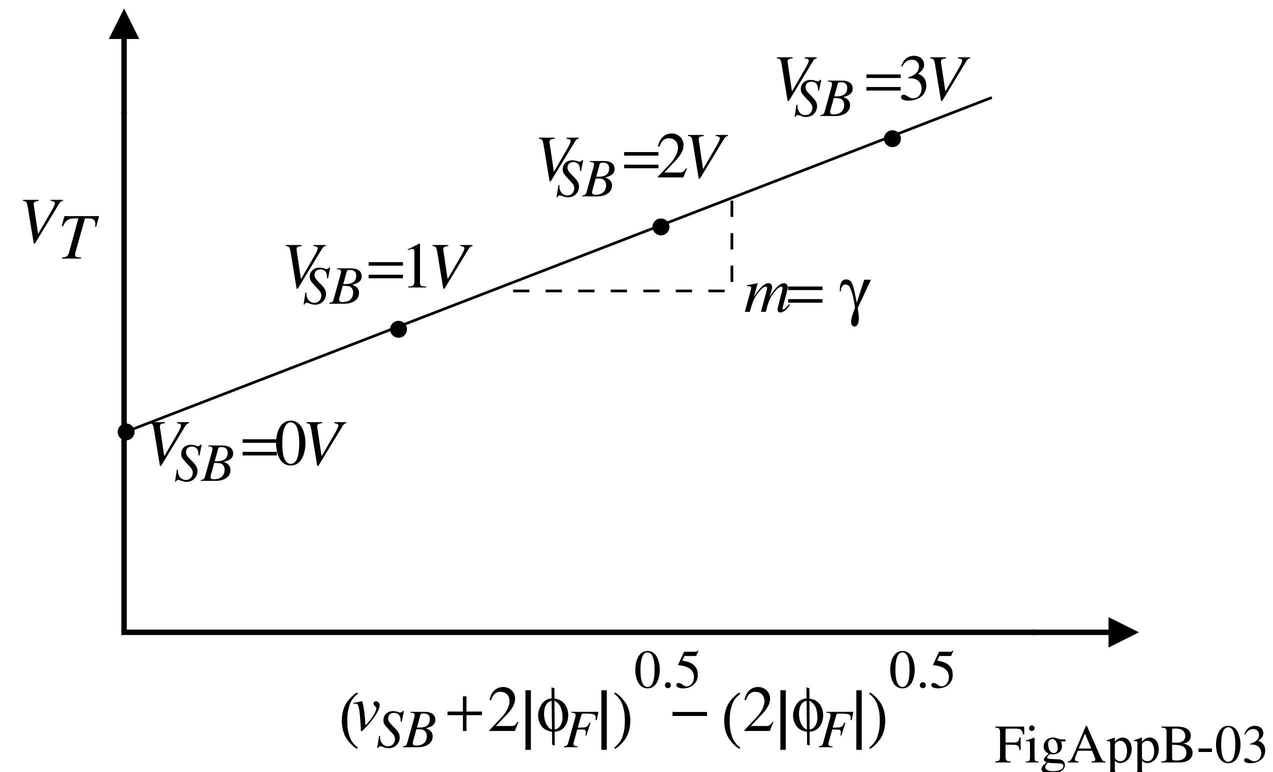
A plot of $\sqrt{i_D}$ versus v_{GS} for different values of v_{SB} used to determine γ is shown below.



By plotting V_T versus x of Eq. (19) one can measure the slope of the best fit line from which the parameter γ can be extracted. In order to do this, V_T must be determined at various values of v_{SB} using the technique previously described.

Illustration of the Procedure for Extracting γ - Continued

Each V_T determined above must be plotted against the v_{SB} term. The result is shown below. The slope m, measured from the best fit line, is the parameter γ.



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Example 3.10-2 – Extraction of the Bulk Threshold Parameter

Using the results from Ex. B-1 and the following transistor data, determine the value of γ using linear regression techniques. Assume that $2|\phi_F|$ is 0.6 volts.

Table 3.10-2 Data for Example 3.10-2.

V_{SB} (V)	V_{GS} (V)	I_D (μA)
1.000	1.400	1.431
1.000	1.600	4.55
1.000	1.800	9.44
1.000	2.000	15.95
2.000	1.700	3.15
2.000	1.900	7.43
2.000	2.10	13.41
2.000	2.30	21.2

Solution

Table B-2 shows data for V_{SB} = 1 volt and V_{SB} = 2 volts. A quick check of the data in this table reveals that $\sqrt{I_D}$ versus V_{GS} is linear and thus may be used in the linear regression analysis. Using the same procedure as in Ex. B-1, the following thresholds are determined: V_{T0} = 0.898 volts (from Ex. B-1), V_T = 1.143 volts (@V_{SB} = 1 V), and V_T = 1.322 V (@V_{SB} = 2 V). Table B-3 gives the value of V_T as a function of $[(2|\phi_F| + V_{SB})^{1/2} - (2|\phi_F|)^{1/2}]$ for the three values of V_{SB}.

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Example 3.10-2 - Continued

Table 3.10-3 Data for Example 3.10-2.

V_{SB} (V)	V_T (V)	$[\sqrt{2\|\phi_F\| + V_{SB}} - \sqrt{2\|\phi_F\|}]$ ($V^{1/2}$)
0.000	0.898	0.000
1.000	1.143	0.490
2.000	1.322	0.838

With these data, linear regression must be performed on the data of V_T versus $[(2|\phi_F| + V_{SB})^{0.5} - (2|\phi_F|)^{0.5}]$. The regression parameters of Eq. (13) are

$$\Sigma x_i y_i = 1.668$$

$$\Sigma x_i y_i = 4.466$$

$$\Sigma x_i^2 = 0.9423$$

$$(\Sigma x_i)^2 = 1.764$$

These values give $m = 0.506 = \gamma$.

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Extraction of the Channel Length Modulation Parameter, λ

The channel length modulation parameter λ should be determined for all device lengths that might be used. For the sake of simplicity, Eq. (2) is rewritten as

$$i_D = i'_D = \lambda' v_{DS} + i'_D \quad (22)$$

which is in the familiar linear form where

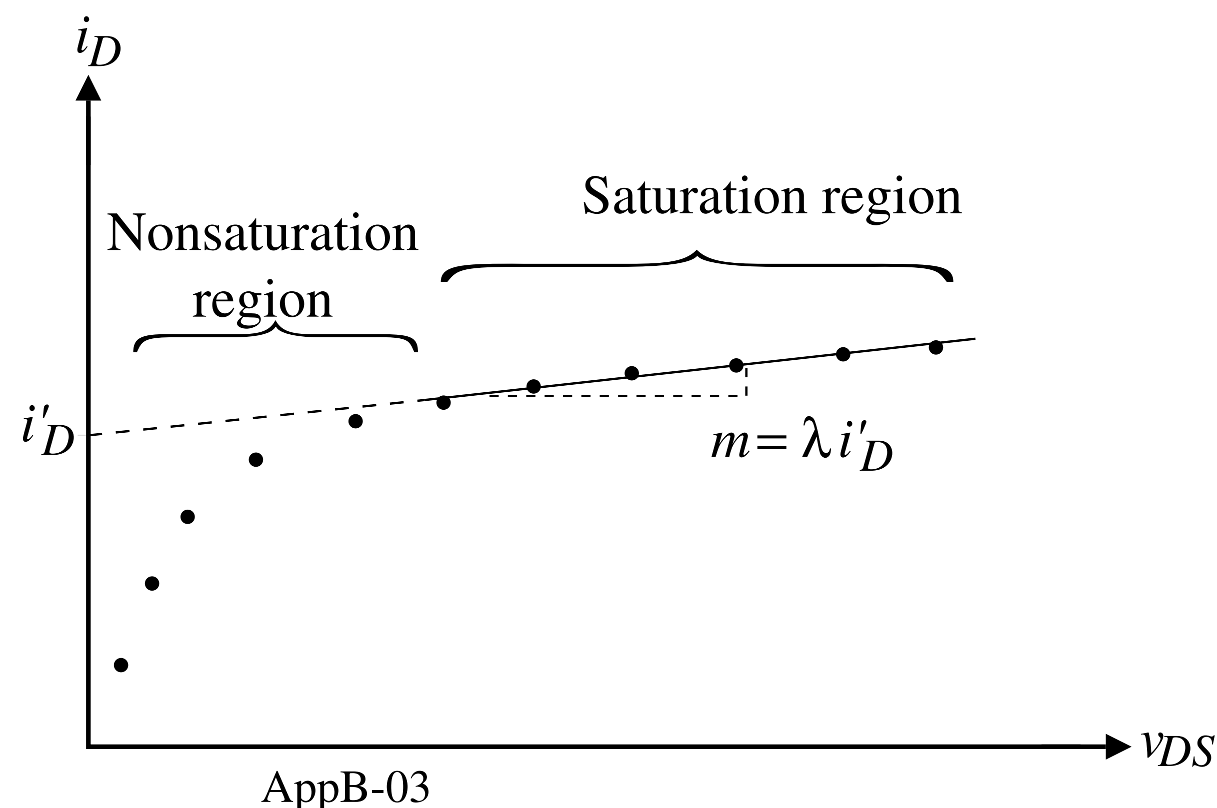
$$y = i_D \text{ (Eq. (2))} \quad 23)$$

$$x = v_{DS} \quad (24)$$

$$m = \lambda i'_D \quad (25)$$

$$b = i'_D \text{ (Eq. (2) with } \lambda = 0) \quad (26)$$

By plotting i_D versus v_{DS}, measuring the slope of the data in the saturation region, and dividing that value by the y-intercept, λ can be determined. The procedure is illustrated in the figure shown.



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Example 3.10-3 – Extraction of the Channel Length Modulation Parameter

Given the data of I_D versus V_{DS} in Table 10.3-4, determine the parameter λ.

Table 10.3-4 Data for Example 3.10-3.

I_D (μA)	39.2	68.2	86.8	94.2	95.7	97.2	98.8	100.3
V_{DS} (V)	0.500	1.000	1.500	2.000	2.50	3.00	3.50	4.00

Solution

We note that the data of Table 3.10-4 covers both the saturation and nonsaturation regions of operation. A quick check shows that saturation is reached near V_{DS} = 2.0 V. To calculate λ, we shall use the data for V_{DS} greater than or equal to 2.5 V. The parameters of the linear regression are

$$x_i y_i = 1277.85 \qquad \sum x_i \sum y_i = 5096.00$$

$$\sum x^2{}_i = 43.5 \qquad (\sum x_i)^2 = 169$$

These values result in $m = \lambda I'_D = 3.08$ and $b = I'_D = 88$, giving $\lambda = 0.035\ \text{V}^{-1}$.

The slope in the saturation region is typically very small, making it necessary to be careful that two data points taken with low resolution are not subtracted (to obtain the slope) resulting in a number that is of the same order of magnitude as the resolution of the data point measured. If this occurs, then the value obtained will have significant and unacceptable error.

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SEC. 3.11 - SUMMARY

- Model philosophy for analog IC design
  Use simple models for design and sophisticated models for verification
- Models have several parts
  Large signal static (dc variables)
  Small signal static (midband gains, resistances)
  Small signal dynamic (frequency response, noise)
  Large signal dynamic (slew rate)
- In addition models may include:
  Temperature
  Noise
  Process variations (Monte Carlo methods)
- Computer models
  Must be numerically efficient
  Quickly derived from new technology
- Analog Design "Tricks"
  Stay away from minimum channel length if possible
    - Larger $r_{ds} \rightarrow$ larger gains
    - Better agreement
  Don't use the computer models for design, rather verification of design

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