CHAPTER 8 - CMOS COMPARATORS

Chapter Outline

SECTION 8.1 - CHARACTERIZATION OF COMPARATORS

Circuit Symbol for a Comparator

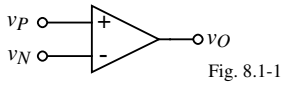


Fig. 8.1-1

Static Characteristics

- Gain
- Output high and low states
- Input resolution
- Offset
- Noise

Dynamic Characteristics

- Propagation delay
- Slew rate

Noninverting and Inverting Comparators

The comparator output is binary with the two-level outputs defined as,

V_{OH} = the high output of the comparator

V_{OL} = the low level output of the comparator

Voltage transfer function of an Noninverting and Inverting Comparator:

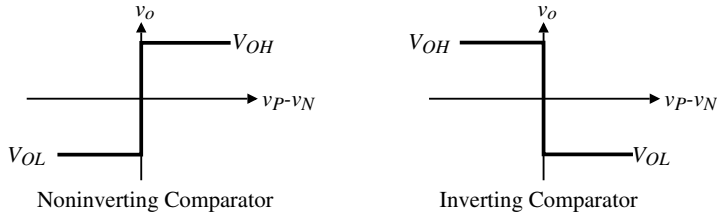


Fig. 8.1-2A

Static Characteristics - Zero-order Model for a Comparator

Voltage transfer function curve:

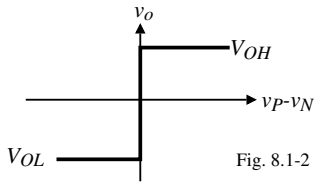
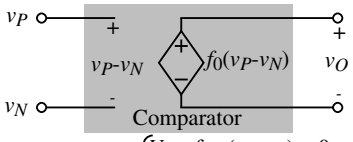


Fig. 8.1-2

Model:



$$f_0(v_P\text{-}v_N) = \begin{cases} V_{OH} \text{ for } (v_P\text{-}v_N) > 0 \\ V_{OL} \text{ for } (v_P\text{-}v_N) < 0 \end{cases}$$

Fig. 8.1-3

$$\text{Gain} = A_v = \lim_{\Delta V \to 0} \frac{V_{OH}\text{-}V_{OL}}{\Delta V}$$ where ΔV is the input voltage change

Static Characteristics - First-Order Model for a Comparator

Voltage transfer curve:

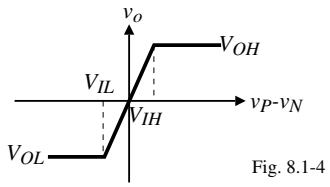


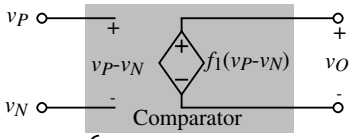
Fig. 8.1-4

where

V_{IH} = smallest input voltage at which the output voltage is V_{OH} (noninverting comparator)

V_{IL} = largest input voltage at which the output voltage is V_{OL} (noninverting comparator)

Model:



$$f_1(v_P\text{-}v_N) = \begin{cases} V_{OH} \text{ for } (v_P\text{-}v_N) > 0 \\ A_v(v_P\text{-}v_N) \text{ for } V_{IL} < (v_P\text{-}v_N) < V_{IH} \\ V_{OL} \text{ for } (v_P\text{-}v_N) < 0 \end{cases}$$

Fig. 8.1-5

The voltage gain is $A_v = \dfrac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}}$

Static Characteristics - First-Order Model including Input Offset Voltage

Voltage transfer curve:

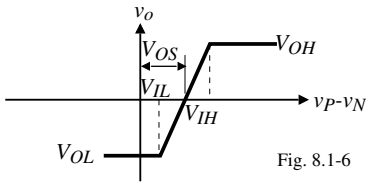


Fig. 8.1-6

V_{OS} = the input voltage necessary to make the output equal $\dfrac{V_{OH}+V_{OL}}{2}$ when $v_P = v_N$.

Model:

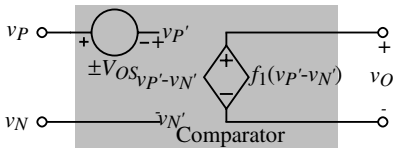


Fig. 8.1-7

Other aspects of the model:

ICMR = input common mode voltage range (all transistors remain in saturation)

R_{in} = input differential resistance

R_{icm} = common mode input resistance

Static Characteristics - Comparator Noise

Noise of a comparator is modeled as if the comparator were biased in the transition region.

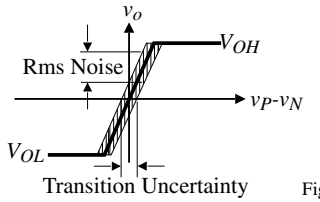


Fig. 8.1-8

Noise leads to an uncertainty in the transition region which causes jitter or phase noise.

Dynamic Characteristics - Propagation Time Delay

Rising propagation delay time:

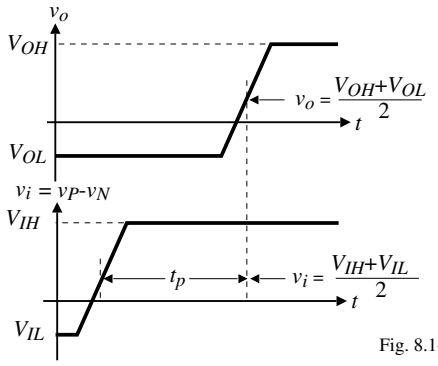


Fig. 8.1-9

Total propagation delay time = $\frac{\text{Rising propagation delay time + Falling propagation delay time}}{2}$

Dynamic Characteristics - Single-Pole Response

Model:

$$A_v(s) = \frac{A_v(0)}{\frac{s}{\omega_c} + 1} = \frac{A_v(0)}{s\tau_c + 1}$$

where

$A_v(0)$ = dc voltage gain of the comparator

$\omega_c = \frac{1}{\tau_c}$ = -3dB frequency of the comparator or the magnitude of the pole

Step Response:

$$v_o(t) = A_v(0)\,[1 - e^{-t/\tau_c}]V_{in}$$

where

V_{in} = the magnitude of the step input.

Dynamic Characteristics - Propagation Time Delay

The rising propagation time delay for a single-pole comparator is:

$$\frac{V_{OH}-V_{OL}}{2} = A_v(0)\,[1 - e^{-t_p/\tau_c}]V_{in} \quad \rightarrow \quad t_p = \tau_c\, ln\left[\frac{1}{1 - \frac{V_{OH}-V_{OL}}{2A_v(0)V_{in}}}\right]$$

Define the minimum input voltage to the comparator as,

$$V_{in}(\text{min}) = \frac{V_{OH}-V_{OL}}{A_v(0)} \quad \rightarrow \quad t_p = \tau_c\, ln\left[\frac{1}{1 - \frac{V_{in}(\text{min})}{2V_{in}}}\right]$$

Define k as the ratio of the input step voltage, V_{in}, to the minimum input voltage, V_{in}(min),

$$k = \frac{V_{in}}{V_{in}(\text{min})} \quad \rightarrow \quad t_p = \tau_c\, ln\left[\frac{2k}{2k-1}\right]$$

Thus, if $k = 1$, $t_p = 0.693\,\tau_c$.

Illustration:

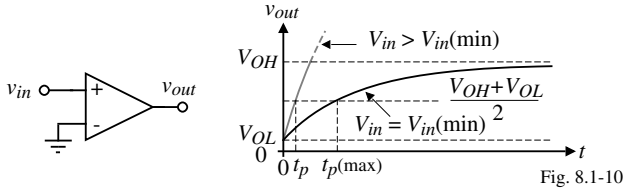


Fig. 8.1-10

Obviously, the more overdrive applied to the input, the smaller the propagation delay time.

Dynamic Characteristics - Slew Rate of a Comparator

If the rate of rise or fall of a comparator becomes large, the dynamics may be limited by the slew rate.

Slew rate comes from the relationship,

$$i = C\frac{dv}{dt}$$

where i is the current through a capacitor and v is the voltage across it.

If the current becomes limited, then the voltage rate becomes limited.

Therefore for a comparator that is slew rate limited we have,

$$t_p = \Delta T = \frac{\Delta V}{SR} = \frac{V_{OH^-} V_{OL}}{2 \cdot SR}$$

where

SR = slew rate of the comparator.

Example 8.1-1 - Propagation Delay Time of a Comparator

Find the propagation delay time of an open loop comparator that has a dominant pole at 10^3 radians/sec, a dc gain of 10^4, a slew rate of 1V/μs, and a binary output voltage swing of 1V. Assume the applied input voltage is 10mV.

Solution

The input resolution for this comparator is $1V/10^4$ or 0.1mV. Therefore, the 10mV input is 100 times larger than v_{in}(min) giving a k of 100. Therefore, we get

$$t_p = \frac{1}{10^3} ln\left(\frac{2 \cdot 100}{2 \cdot 100\text{-}1}\right) = 10^{-3}\, ln\left(\frac{200}{199}\right) = 5.01\mu s$$

For slew rate considerations, we get

$$t_p = \frac{1}{2 \cdot 1 x 10^6} = 0.5\mu s$$

Therefore, the propagation delay time for this case is the larger or 5.01μs.

SECTION 8.2 - TWO-STAGE, OPEN-LOOP COMPARATORS

Two-Stage Comparator

An important category of comparators are those which use a high-gain stage to drive their outputs between V_{OH} and V_{OL} for very small input voltage changes.

The two-stage op amp without compensation is an excellent implementation of a high-gain, open-loop comparator.

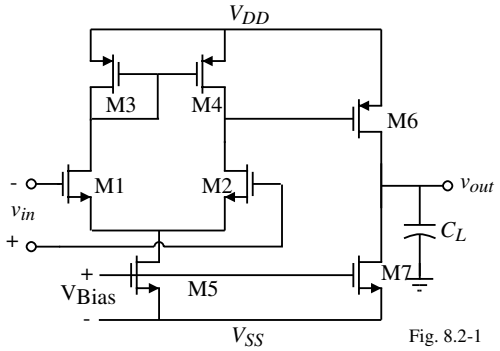


Fig. 8.2-1

Performance of the Two-Stage, Open-Loop Comparator

We know that the performance should be similar to the uncompensated two-stage op amp of Chapter 6.

Emphasis on comparator performance:

- Maximum output voltage

$$V_{OH} = V_{DD} - (V_{DD}-V_{G6}(\min)-|V_{TP}|)\left[1 - \sqrt{1 - \frac{8I_7}{\beta_6(V_{DD}-V_{G6}(\min)-|V_{TP}|)^2}}\right]$$

- Minimum output voltage

$$V_{OL} = V_{SS}$$

- Small-signal voltage gain

$$A_v(0) = \left(\frac{g_{m1}}{g_{ds2}+g_{ds4}}\right)\left(\frac{g_{m6}}{g_{ds6}+g_{ds7}}\right)$$

- Poles

  Input:

$$p_1 = \frac{-1}{C_I(g_{ds2}+g_{ds4})}$$

  Output:

$$p_2 = \frac{-1}{C_{II}(g_{ds6}+g_{ds7})}$$

- Frequency response

$$A_v(s) = \frac{A_v(0)}{\left(\frac{s}{p_1}+1\right)\left(\frac{s}{p_2}+1\right)}$$

Example 8.2-1 - Performance of a Two-Stage Comparator

Evaluate V_{OH}, V_{OL}, $A_v(0)$, $V_{in}(\min)$, p_1, p_2, for the two-stage comparator shown in Fig. 8.2-1. Assume that this comparator is the circuit of Ex. 6.3-1 with no compensation capacitor, C_c, and the minimum value of $V_{G6} = 0$V. Also, assume that $C_I = 0.2$pF and $C_{II} = 5$pF.

Solution

Using the above relations, we find that

$$V_{OH} = 2.5 - (2.5\text{-}0\text{-}0.7)\left[1 - \sqrt{1 - \frac{8\cdot 234\text{x}10^{-6}}{50\text{x}10^{-6}\cdot 38(2.5\text{-}0\text{-}0.7)^2}}\right] = 2.2\text{V}$$

The value of V_{OL} is -2.5V. The gain was evaluated in Ex. 6.3-1 as $A_v(0) = 7696$. Therefore, the input resolution is

$$V_{in}(\min) = \frac{V_{OH}\text{-}V_{OL}}{A_v(0)} = \frac{4.7\text{V}}{7696} = 0.611\text{mV}$$

Next, we find the poles of the comparator, p_1 and p_2. From Ex. 6.3-1 we find that

$$p_1 = \frac{g_{ds2} + g_{ds4}}{C_I} = \frac{15\text{x}10^{-6}(0.04+0.05)}{0.2\text{x}10^{-12}} = 6.75\text{x}10^6 \text{ (1.074MHz)}$$

and

$$p_2 = \frac{g_{ds6} + g_{ds7}}{C_{II}} = \frac{95\text{x}10^{-6}(0.04+0.05)}{5\text{x}10^{-12}} = 1.71\text{x}10^6 \text{ (0.272MHz)}$$

Linear Step Response of the Two-Stage Comparator

The step response of a circuit with two real poles ($p_1 \neq p_2$) is,

$$v_{out}(t) = A_v(0)V_{in}\left[1 + \frac{p_2 e^{-tp_1}}{p_1\text{-}p_2} - \frac{p_1 e^{-tp_2}}{p_1\text{-}p_2}\right]$$

Normalizing gives,

$$v_{out}'(t_n) = \frac{v_{out}(t)}{A_v(0)V_{in}} = 1 - \frac{m}{m\text{-}1}e^{-t_n} + \frac{1}{m\text{-}1}e^{-mt_n} \qquad \text{where} \quad m = \frac{p_2}{p_1} \neq 1 \quad \text{and} \quad t_n = tp_1 = \frac{t}{\tau_1}$$

If $p_1 = p_2$ ($m = 1$), then

$$v_{out}'(t_n) = 1 - p_1 e^{-t_n} - \frac{t_n}{p_1}e^{-t_n} = 1 - e^{-t_n} - t_n e^{-t_n} \qquad \text{where } p_1 = 1.$$

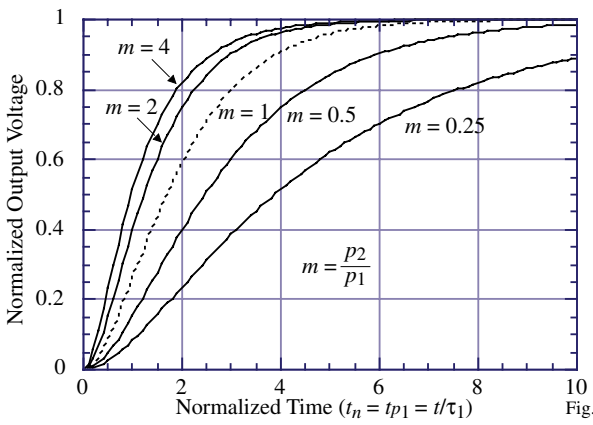


Fig. 8.2-2

Linear Step Response of the Two-Stage Comparator - Continued

The above results are valid as long as the slope of the linear response does not exceed the slew rate.

- Slope at $t = 0$ is zero
- Maximum slope occurs at ($m \neq 1$)

$$t_n(\max) = \frac{ln(m)}{m\text{-}1}$$

and is

$$\frac{dv_{out}'(t_n(\max))}{dt_n} = \frac{m}{m\text{-}1}\left[\exp\left(\frac{-ln(m)}{m\text{-}1}\right) - \exp\left(-m\frac{ln(m)}{m\text{-}1}\right)\right]$$

- For the two-stage comparator using NMOS input transistors, the slew rate is

$$SR^- = \frac{I_7}{C_{II}}$$

$$SR^+ = \frac{I_6\text{-}I_7}{C_{II}} = \frac{\beta_6(V_{DD}\text{-}V_{G6}(\min)\text{-}|V_{TP}|)^2 - I_7}{C_{II}}$$

Example 8.2-2 - Step Response of Ex. 8.2-1

Find the maximum slope of Ex. 8.2-1 and the time at which it occurs if the magnitude of the input step is $v_{in}(\min)$. If the dc bias current in M7 is 100μA, at what value of load capacitance, C_L would the transient response become slew limited? If the magnitude of the input step is $100v_{in}(\min)$, what would be the new value of C_L at which slewing would occur?

Solution

The poles of the comparator were given in Ex. 8.2-1 as $p_1 = -6.75\text{x}10^6$ rads/sec. and $p_2 = -1.71\text{x}10^6$ rads/sec. This gives a value of $m = 0.253$. From the previous expressions, the maximum slope occurs at $t_n(\max) = 1.84$ secs. Dividing by $|p_1|$ gives $t(\max) = 0.272$μs. The slope of the transient response at this time is found as

$$\frac{dv_{out}'(t_n(\max))}{dt_n} = -0.338[\exp(-1.84) - \exp(-0.253\cdot 1.84)] = 0.159 \text{ V/sec}$$

Multiplying the above by $|p_1|$ gives

$$\frac{dv_{out}'(t(\max))}{dt} = 1.072\text{V/μs}$$

Therefore, if the slew rate of the comparator is less than 1.072V/μs, the transient response will experience slewing. Also, if the load capacitance, C_L, becomes larger than 100μA/1.072V/μs or 93.3pF, the comparator will experience slewing.

If the comparator is overdriven by a factor of $100v_{in}(\min)$, then we must unnormalize the output slope as follows.

$$\frac{dv_{out}'(t(\max))}{dt} = \frac{v_{in}}{v_{in}(\min)}\frac{dv_{out}'(t(\max))}{dt} = 100\cdot 1.072\text{V/μs} = 107.2\text{V/μs}$$

Therefore, the comparator will now slew with a load capacitance of 0.933pF. For large overdrives, the comparator will generally experience slewing.

Propagation Delay Time (Non-Slew)

To find t_p, we want to set $0.5(V_{OH}\text{-}V_{OL})$ equal to $v_{out}(t_n)$. However, $v_{out}(t_n)$ is given as

$$v_{out}(t_n) = A_v(0)V_{in}\left[1 - \frac{m}{m\text{-}1}e^{-t_n} + \frac{1}{m\text{-}1}e^{-mt_n}\right]$$

which can't be easily solved so approximating the step response as a power series gives

$$v_{out}(t_n) \approx A_v(0)V_{in}\left[1 - \frac{m}{m\text{-}1}\left(1\text{-}t_n + \frac{t_n^2}{2} + \cdots\right) + \frac{1}{m\text{-}1}\left(1\text{-}mt_n + \frac{m^2t_n^2}{2} + \cdots\right)\right] \approx \frac{mt_n^2A_v(0)V_{in}}{2}$$

Therefore, set $v_{out}(t_n) = 0.5(V_{OH}\text{-}V_{OL})$

$$\frac{V_{OH}+V_{OL}}{2} \approx \frac{mt_{pn}^2A_v(0)V_{in}}{2}$$

or

$$t_{pn} \approx \sqrt{\frac{V_{OH}+V_{OL}}{mA_v(0)V_{in}}} = \sqrt{\frac{V_{in}(\min)}{mV_{in}}} = \frac{1}{\sqrt{mk}}$$

This approximation is particularly good for large values of k.

Example 8.2-3 - Propagation Delay Time of a Two-Pole Comparator (Non-Slew)

Find the propagation time delay of the comparator of Ex. 8.2-1 if V_{in} = 10mV, 100mV and 1V.

Solution

From Ex. 8.2-1 we know that $V_{in}(\min)$ = 0.611mV and m = 0.253. For V_{in} = 10mV, k = 16.366 which gives $t_{pn} \approx 0.491$. The propagation time delay is equal to $0.491/6.75\text{x}10^6$ or 72.9nS. This corresponds well with Fig. 8.2-2 where the normalized propagation time delay is the time at which the amplitude is $1/2k$ or 0.031 which corresponds to t_{pn} of approximately 0.5. Similarly, for V_{in} = 100mV and 1V we get a propagation time delay of 23ns and 7.3ns, respectively.

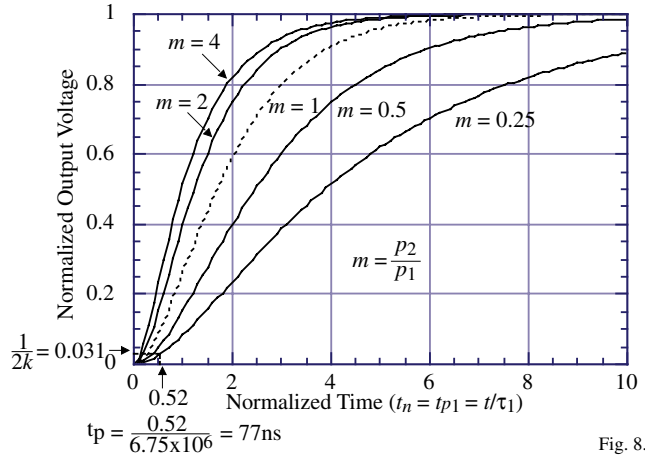


Fig. 8.2-2A

Initial Operating States for the Two-Stage, Open-Loop Comparator

What are the initial operating states for the following comparator?

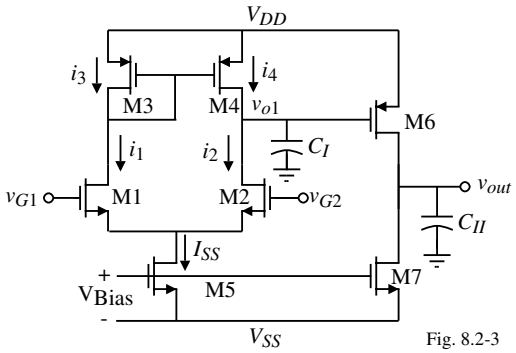


Fig. 8.2-3

1.) Assume $v_{G2} = V_{REF}$ and $v_{G1} > V_{REF}$ with $i_1 < I_{SS}$ and $i_2 > 0$.

Initially, $i_4 > i_2$ and v_{o1} increases, M4 becomes active and i_4 decreases until $i_3 = i_4$. v_{o1} is in the range of,

$$V_{DD} - V_{SD4}(\text{sat}) < v_{o1} < V_{DD}, \qquad v_{G1} > V_{REF},\ i_1 < I_{SS} \text{ and } i_2 > 0$$

and the value of v_{out} is

$$v_{out} \approx V_{SS} \qquad v_{G1} > V_{REF},\ i_1 < I_{SS} \text{ and } i_2 > 0$$

2.) Assume $v_{G2} = V_{REF}$ and $v_{G1} >> V_{REF}$, therefore $i_1 = I_{SS}$ and $i_2 = 0$ which gives

$$v_{o1} = V_{DD} \qquad \text{and} \qquad v_{out} = V_{SS}$$

Initial Operating States - Continued

3.) Assume $v_{G2} = V_{REF}$ and $v_{G1} < V_{REF}$ with $i_1 > 0$ and $i_2 < I_{SS}$.

Initially, $i_4 < i_2$ and v_{o1} decreases. When $v_{o1} \le V_{REF} - V_{TN}$, M2 becomes active and i_2 decreases. When $i_1 = i_2 = I_{SS}/2$ the circuit stabilizes and v_{o1} is in the range of,

$$V_{REF} - V_{GS2} < v_{o1} < V_{REF} - V_{GS2} + V_{DS2}(\text{sat})$$

or

$$V_{S2} < v_{o1} < V_{S2} + V_{DS2}(\text{sat}), \qquad v_{G1} < V_{G2},\ i_1 > 0 \text{ and } i_2 < I_{SS}$$

For the above conditions,

$$v_{out} = V_{DD} - (V_{DD} - v_{o1} - |V_{TP}|)\left[1 - \sqrt{1 - \frac{\beta_7 I_{SS}}{\beta_5\beta_6(V_{DD} - v_{o1} - |V_{TP}|)^2}}\right]$$

4.) Assume $v_{G2} = V_{REF}$ and $v_{G1} << V_{REF}$, therefore $i_2 = I_{SS}$ and $i_1 = 0$.

Same as in 3.) but now as v_{o1} approaches v_{S2} with $I_{SS}/2$ flowing, the value of v_{GS2} becomes larger and M5 becomes active and I_{SS} decreases. In the limit, $I_{SS} \to 0$, $v_{DS2} \approx 0$ and $v_{DS5} \approx 0$ resulting in

$$v_{o1} \approx V_{SS} \qquad \text{and} \qquad v_{out} = V_{DD} - (V_{DD} - V_{SS} - |V_{TP}|)\left[1 - \sqrt{1 - \frac{\beta_7 I_{SS}}{\beta_5\beta_6(V_{DD} - V_{SS} - |V_{TP}|)^2}}\right]$$

Initial Operating States - Continued

5.) Assume $v_{G1} = V_{REF}$ and $v_{G2} > V_{REF}$ with $i_2 < I_{SS}$ and $i_1 > 0$.

Initially, $i_4 < i_2$ and v_{o1} falls, M2 becomes active and i_2 decreases until $i_1 = i_2 = I_{SS}/2$. Therefore,

$$V_{REF} - V_{GS2}(I_{SS}/2) < v_{o1} < V_{REF} - V_{GS2}(I_{SS}/2) + V_{DS2}(\text{sat})$$

or

$$V_{S2}(I_{SS}/2) < v_{o1} < V_{S2}(I_{SS}/2) + V_{DS2}(\text{sat}), \qquad v_{G2} > V_{REF},\ i_1 > 0 \text{ and } i_2 < I_{SS}$$

and the value of v_{out} is

$$v_{out} = V_{DD} - (V_{DD} - v_{o1} - |V_{TP}|)\left[1 - \sqrt{1 - \frac{\beta_7 I_{SS}}{\beta_5\beta_6(V_{DD} - v_{o1} - |V_{TP}|)^2}}\right]$$

6.) Assume that $v_{G1} = V_{REF}$ and $v_{G2} >> V_{REF}$. When the source voltage of M1 or M2 causes M5 to be active, then I_{SS} decreases and

$$v_{o1} \approx V_{SS}$$

and

$$v_{out} = V_{DD} - (V_{DD} - V_{SS} - |V_{TP}|)\left[1 - \sqrt{1 - \frac{\beta_7 I_{SS}}{\beta_5\beta_6(V_{DD} - V_{SS} - |V_{TP}|)^2}}\right]$$

7.) Assume $v_{G1} = V_{REF}$ and $v_{G2} < V_{REF}$ and $i_1 < I_{SS}$ and $i_2 > 0$. Consequently, $i_4 > i_2$ which causes v_{o1} to increase. When M4 becomes active i_4 decreases until $i_2 = i_4$ at which v_{o1} stabilizes at

$$V_{DD} - V_{SD4}(\text{sat}) < v_{o1} < V_{DD}, \qquad v_{G2} < V_{REF},\ i_1 < I_{SS} \text{ and } i_2 > 0$$

M6 will be off under these conditions and $v_{out} \approx V_{SS}$.

Initial Operating States - Continued

8.) Finally if $v_{G2} << V_{REF}$, then $i_1 = I_{SS}$ and $i_2 = 0$ and

$$v_{o1} \approx V_{DD} \qquad \text{and} \qquad v_{out} \approx V_{SS}.$$

Summary of the Initial Operating States of the Two-Stage, Open-Loop Comparator using a N-channel, Source-coupled Input Pair:

Conditions	Initial State of v_{o1}	Initial State of v_{out}
$v_{G1} > V_{G2}$, $i_1 < I_{SS}$ and $i_2 > 0$	$V_{DD} - V_{SD4}(\text{sat}) < v_{o1} < V_{DD}$	V_{SS}
$v_{G1} >> V_{G2}$, $i_1 = I_{SS}$ and $i_2 = 0$	V_{DD}	V_{SS}
$v_{G1} < V_{G2}$, $i_1 > 0$ and $i_2 < I_{SS}$	$v_{o1} = V_{G2} - V_{GS2,\text{act}}(I_{SS}/2)$, $\approx V_{SS}$ if M5 act.	Eq. (19), Sec. 5.1 for PMOS
$v_{G1} << V_{G2}$, $i_1 > 0$ and $i_2 < I_{SS}$	V_{SS}	Eq. (19), Sec. 5.1 for PMOS
$v_{G2} > V_{G1}$, $i_1 > 0$ and $i_2 < I_{SS}$	$V_{S2}(I_{SS}/2) < v_{o1} < V_{S2}(I_{SS}/2) + V_{DS2}(\text{sat})$	Eq. (19), Sec. 5.1 for PMOS
$v_{G2} >> V_{G1}$, $i_1 > 0$ and $i_2 < I_{SS}$	$V_{G1} - V_{GS1}(I_{SS}/2)$, $\approx V_{SS}$ if M5 active	Eq. (19), Sec. 5.1 for PMOS
$v_{G2} < V_{G1}$, $i_1 < I_{SS}$ and $i_2 > 0$	$V_{DD} - V_{SD4}(\text{sat}) < v_{o1} < V_{DD}$	V_{SS}
$v_{G2} << V_{G1}$, $i_1 << I_{SS}$ and $i_2 > 0$	V_{DD}	V_{SS}

Trip Point of an Inverter

In order to determine the propagation delay time, it is necessary to know when the second stage of the two-stage comparator begins to "turn on".

Second stage:

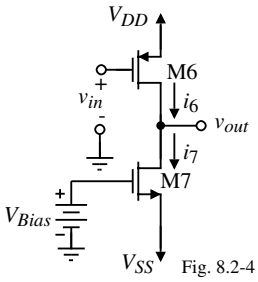


Fig. 8.2-4

Trip point:

Assume that M6 and M7 are saturated. (We know that the steepest slope occurs for this condition.)

Equate i_6 to i_7 and solve for v_{in} which becomes the trip point.

$$\therefore \qquad v_{in} = V_{TRP} = V_{DD} - |V_{TP}| - \sqrt{\frac{K_N(W_7/L_7)}{K_P(W_6/L_6)}}(V_{Bias} - V_{SS} - V_{TN})$$

Example:

If $W_7/L_7 = W_6/L_6$, $V_{DD} = 2.5\text{V}$, $V_{SS} = -2.5\text{V}$, and $V_{Bias} = 0\text{V}$ the trip point for the circuit above is

$$V_{TRP} = 2.5 - 0.7 - \sqrt{110/50}\,(0 + 2.5 - 0.7) = -0.870\text{V}$$

Propagation Delay Time of a Slewing, Two-Stage, Open-Loop Comparator

Previously we calculated the propagation delay time for a nonslewing comparator.

If the comparator slews, then the propagation delay time is found from

$$i_i = C_i\frac{dv_i}{dt_i} = C_i\frac{\Delta v_i}{\Delta t_i}$$

where

C_i is the capacitance to ground at the output of the i-th stage

The propagation delay time of the i-th stage is,

$$t_i = \Delta t_i = C_i\frac{\Delta V_i}{I_i}$$

The propagation delay time is found by summing the delays of each stage.

$$t_p = t_1 + t_2 + t_3 + \cdots$$

Example 8.2-5 - Calculation of the Propagation Time Delay of a Two-Stage, Open-Loop Comparator

For the two-stage comparator shown assume that C_I = 0.2pF and C_{II} = 5pF. Also, assume that v_{G1} = 0V and that v_{G2} has the waveform shown. If the input voltage is large enough to cause slew to dominate, find the propagation time delay of the rising and falling output of the comparator and give the propagation time delay of the comparator.

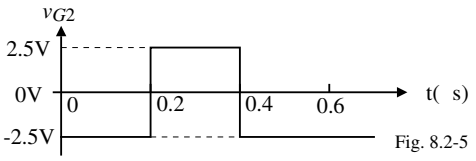


Fig. 8.2-5

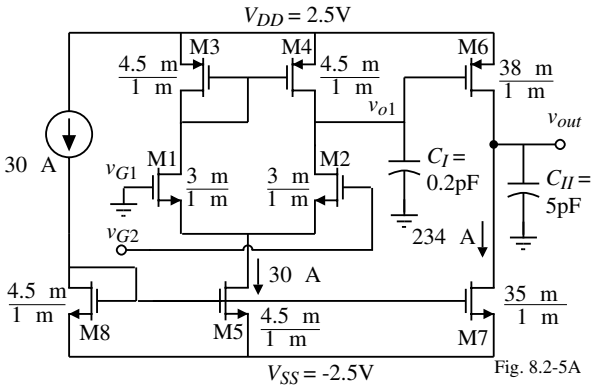


Fig. 8.2-5A

Solution

The total delay will be given as the sum of the first and second stage delays, t_1 and t_2, respectively. First, consider the change of v_{G2} from -2.5V to 2.5V at 0.2μs. From Table 8.2-1, the last row, the initial states of v_{o1} and v_{out} are +2.5V and -2.5V, respectively. To find the falling delay of the first stage, t_{f1}, requires C_I, ΔV_{o1}, and I_5. C_I = 0.2pF, I_5 = 30μA and ΔV_1 can be calculated by finding the trip point of the output stage by setting the current of M6 when saturated equal to 234μA.

$$\frac{\beta_6}{2}(V_{SG6}-|V_{TP}|)^2 = 234\mu A \;\rightarrow\; V_{SG6} = 0.7 + \sqrt{\frac{234\cdot 2}{110\cdot 38}} = 1.035V$$

Therefore, the trip point of the second stage is V_{TRP2} = 2.5 - 1.035 = 1.465V

Example 8.2-5 - Continued

Therefore, ΔV_1 = 2.5V - 1.465V = V_{SG6} = 1.035V. Thus the falling propagation time delay of the first stage is

$$t_{fo1} = 0.2\text{pF}\left(\frac{1.035V}{30\mu A}\right) = 6.9\text{ns}$$

The rising propagation time delay of the second stage requires the knowledge of C_{II}, ΔV_{out}, and I_6. C_{II} is given as 5pF, ΔV_{out} = 2.5V (assuming the trip point of the circuit connected to the output of the comparator is 0V), and I_6 can be found as follows. When the gate of M6 is at 1.465V, the current is 234μA. However, the output of the first stage will continue to fall so what value should be used for the gate in order to calculate I_6? The lowest value of V_{G6} is given as

$$V_{G6} = V_{G1} - V_{GS1}(I_{SS}/2) + V_{DS2} \approx -V_{GS1}(I_{SS}/2) = -0.7 - \sqrt{\frac{2\cdot 15}{110\cdot 3}} = -1.00V$$

Let us take the approximate value of V_{G6} as midway between 1.465V and -1.00V which is 0.232V. Therefore V_{SG6} = 2.27V and the value of I_6 is

$$I_6 = \frac{\beta_6}{2}(V_{SG6}-|V_{TP}|)^2 = \frac{38\cdot 50}{2}(2.27 - 0.7)^2 = 2{,}342\mu A$$

which is a reminder that the active transistor can generally sink or source more current than the fixed transistor in the class-A inverting stage. The rising propagation time delay for the output can expressed as

$$t_{rout} = 5\text{pF}\left(\frac{2.5V}{2{,}342\mu A - 234\mu A}\right) = 5.93\text{ns}$$

Thus the total propagation time delay of the rising output of the comparator is approximately 12.8ns and most of this delay is attributable to the first stage.

Example 8.2-5 - Continued

Next consider the change of v_{G2} from 2.5V to -2.5V which occurs at 0.4μs. We shall assume that v_{G2} has been at 2.5V long enough for the conditions of Table 8.2-1 to be valid. Therefore, $v_{o1} \approx$ 0V-V_{GS1}(30μA) = -1.13V and $v_{out} \approx V_{DD}$. Rather than use Eq. (19) of Sec. 5.1 we have assumed that v_{out} is approximately V_{DD}. The propagation time delays for the first and second stages are calculated as

$$t_{ro1} = 0.2\text{pF}\left(\frac{1.465\text{V}-(-1.13\text{V})}{30\mu\text{A}}\right) = 17.3\text{ns} \qquad t_{fout} = 5\text{pF}\left(\frac{2.5\text{V}}{234\mu\text{A}}\right) = 53.42\text{ns}$$

The total propagation time delay of the falling output is 70.72ns. Taking the average of the rising and falling propagation time delays gives a propagation time delay for this two-stage, open-loop comparator of about 41.76ns. These values compare favorably with the simulation of the comparator.

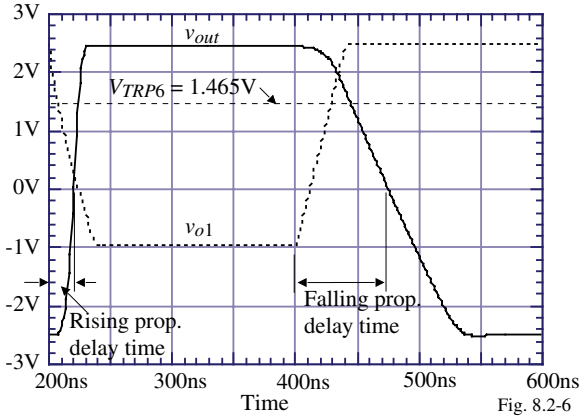


Fig. 8.2-6

Design of a Two-Stage, Open-Loop Comparator

Table 8.2-2 Design of the Two-Stage, Open-Loop Comparator of Fig. 8.2-3 for a Linear Response.

Specifications: t_p, C_{II}, V_{in}(min), V_{OH}, V_{OL}, V_{icm}^+, V_{icm}^-, and overdrive Constraints: Technology, V_{DD} and V_{SS}

Step	Design Relationships	Comments
1	$\lvert p_I\rvert = \lvert p_{II}\rvert = \frac{1}{t_p\sqrt{mk}}$, and $I_7 = I_6 = \frac{\lvert p_{II}\rvert C_{II}}{\lambda_N+\lambda_P}$	Choose $m = 1$
2	$\frac{W_6}{L_6} = \frac{2\cdot I_6}{K_P'(V_{SD6}(\text{sat}))^2}$ and $\frac{W_7}{L_7} = \frac{2\cdot I_7}{K_N'(V_{DS7}(\text{sat}))^2}$	$V_{SD6}(\text{sat}) = V_{DD}-V_{OH}$ $V_{DS7}(\text{sat}) = V_{OL} - V_{SS}$
3	Guess C_I as 0.1pF to 0.5pF $\therefore I_5 = I_7\frac{2C_I}{C_{II}}$	A result of choosing $m = 1$. Will check C_I later
4	$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{I_5}{K_P'(V_{SG3}-\lvert V_{TP}\rvert)^2}$	$V_{SG3} = V_{DD}-V_{icm}^+ + V_{TN}$
5	$g_{m1} = \frac{A_v(0)(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})}{g_{m6}}$ $\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}^2}{K_N I_5}$	$g_{m6} = \sqrt{\frac{2K_P'W_6I_6}{L_6}}$ $A_v(0) = \frac{V_{OH}+V_{OL}}{V_{in}(\text{min})}$
6	Find C_I and check assumption $C_I = C_{gd2}+C_{gd4}+C_{gs6}+C_{bd2}+C_{bd4}$	If C_I is greater than the guess in step 3, then increase C_I and repeat steps 4 through 6
7	$V_{DS5}(\text{sat}) = V_{icm}^- - V_{GS1} - V_{SS}$ $\frac{W_5}{L_5} = \frac{2\cdot I_5}{K_N'(V_{DS5}(\text{sat}))^2}$	If V_{DS5}(sat) is less than 100mV, increase W_1/L_1.

Example 8.2-6 - Design of the Two-Stage, Open-Loop Comparator of Fig. 8.2-3 for a Linear Response.

Assume the specifications of the comparator shown are given below.

t_p = 50ns V_{OH} = 2V V_{OL} = -2V

V_{DD} = 2.5V V_{SS} = -2.5V C_{II} = 5pF

V_{in}(min) = 1mV V_{icm}^+ = 2V V_{icm}^- = -1.25V

Also assume that the overdrive will be a factor of 10. Use this architecture to achieve the above specifications and assume that all channel lengths are to be 1µm.

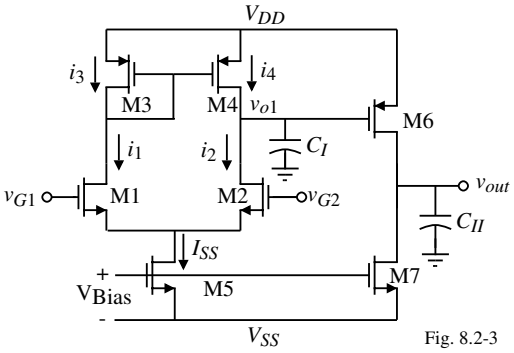


Fig. 8.2-3

Solution

Following the procedure outlined in Table 8.2-2, we choose m = 1 to get

$$|p_I| = |p_{II}| = \frac{10^9}{50\sqrt{10}} = 6.32\text{x}10^6 \text{ rads/sec}$$

This gives

$$I_6 = I_7 = \frac{6.32\text{x}10^6 \cdot 5\text{x}10^{-12}}{0.04+0.05} = 351\mu\text{A} \quad \rightarrow \quad I_6 = I_7 = 400\mu\text{A}$$

Therefore,

$$\frac{W_6}{L_6} = \frac{2\cdot 400}{(0.5)^2\cdot 50} = 64 \quad \text{and} \quad \frac{W_7}{L_7} = \frac{2\cdot 400}{(0.5)^2\cdot 110} = 29$$

Example 8.2-6 - Continued

Next, we guess C_I = 0.2pF. This gives I_5 = 32µA and we will increase it to 40µA for a margin of safety. Step 4 gives V_{SG3} as 1.2V which results in

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{40}{50(1.2\text{-}0.7)^2} = 3.2 \quad \rightarrow \quad \frac{W_3}{L_3} = \frac{W_4}{L_4} = 4$$

The desired gain is found to be 4000 which gives an input transconductance of

$$g_{m1} = \frac{4000\cdot 0.09\cdot 20}{44.44} = 162\mu\text{S}$$

This gives the W/L ratios of M1 and M2 as

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{(162)^2}{110\cdot 40} = 5.96 \quad \rightarrow \quad \frac{W_1}{L_1} = \frac{W_2}{L_2} = 6$$

To check the guess for C_I we need to calculate it which is done as

$$C_I = C_{gd2}+C_{gd4}+C_{gs6}+C_{bd2}+C_{bd4} = 0.9\text{fF}+1.3\text{fF}+119.5\text{fF}+20.4\text{fF}+36.8\text{fF} = 178.9\text{fF}$$

which is less than what was guessed so we will make no changes.

Example 8.2-6 - Continued

Finally, the *W*/*L* value of M5 is found by finding V_{GS1} as 0.946V which gives V_{DS5}(sat) = 0.304V. This gives

$$\frac{W_5}{L_5} = \frac{2 \cdot 40}{(0.304)^2 \cdot 110} = 7.87 \approx 8$$

Obviously, M5 and M7 cannot be connected gate-gate and source-source. The value of I_5 and I_7 must be derived separately as illustrated below. The *W* values are summarized below assuming that all channel lengths are 1μm.

$W_1 = W_2 = 6\mu m$ $W_3 = W_4 = 4\mu m$ $W_5 = 8\mu m$

$W_6 = 64\mu m$ $W_7 = 29\mu m$

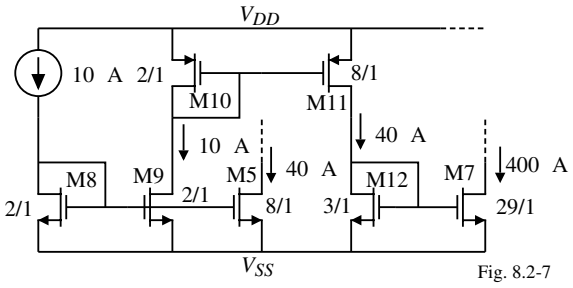


Fig. 8.2-7

Design of a Two-Stage Comparator for a Slewing Response

Table 8.2-3 Design of the Two-Stage, Open-Loop Comparator of Fig. 8.2-3 for a Slewing Response.

Specifications: t_p, C_{II}, V_{in}(min), V_{OH}, V_{OL}, V_{icm}^+, V_{icm}^- Constraints: Technology, V_{DD} and V_{SS}

Step	Design Relationships	Comments
1	$I_7 = I_6 = C_{II}\frac{dv_{out}}{dt} = \frac{C_{II}(V_{OH}-V_{OL})}{t_p}$	Assume the trip point of the output is $(V_{OH}-V_{OL})/2$.
2	$\frac{W_6}{L_6} = \frac{2 \cdot I_6}{K_P'(V_{SD6}(sat))^2}$ and $\frac{W_7}{L_7} = \frac{2 \cdot I_7}{K_N'(V_{DS7}(sat))^2}$	$V_{SD6}(sat) = V_{DD}-V_{OH}$ $V_{DS7}(sat) = V_{OL} - V_{SS}$
3	Guess C_I as 0.1pF to 0.5pF $\quad \therefore I_5 = I_7\frac{2C_I}{C_{II}}$	Typically 0.1pf<C_I<0.5pF
4	$I_5 = C_I\frac{dv_{o1}}{dt} \approx \frac{C_I(V_{OH}-V_{OL})}{t_p}$	Assume that v_{o1} swings between V_{OH} and V_{OL}.
5	$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{I_5}{K_P'(V_{SG3}-\lvert V_{TP}\rvert)^2}$	$V_{SG3} = V_{DD}-V_{icm}^+ + V_{TN}$
6	$g_{m1} = \frac{A_v(0)(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})}{g_{m6}}$ $\quad \frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}^2}{K_N I_5}$	$g_{m6} = \sqrt{\frac{2K_P'W_6I_6}{L_6}}$ $\quad A_v(0) = \frac{V_{OH}+V_{OL}}{V_{in}(min)}$
7	Find C_I and check assumption $C_I = C_{gd2}+C_{gd4}+C_{gs6}+C_{bd2}+C_{bd4}$	If C_I is greater than the guess in step 3, increase the value of C_I and repeat steps 4 through 6
8	$V_{DS5}(sat) = V_{icm}^- - V_{GS1} - V_{SS}$ $\frac{W_5}{L_5} = \frac{2 \cdot I_5}{K_N'(V_{DS5}(sat))^2}$	If V_{DS5}(sat) is less than 100mV, increase W_1/L_1.

Example 8.2-7 - Design of the Two-Stage, Open-Loop Comparator for a Slewing Response

Assume the specifications of Fig. 8.2-3 are given below.

t_p = 50ns V_{OH} = 2V V_{OL} = -2V

V_{DD} = 2.5V V_{SS} = -2.5V C_{II} = 5pF

V_{in}(min) = 1mV V_{icm}^+ = 2V V_{icm}^- = -1.25V

Design a two-stage, open-loop comparator using the circuit of Fig. 8.2-3 to the above specifications and assume all channel lengths are to be 1µm.

Solution

Following the procedure outlined in Table 8.2-3, we calculate I_6 and I_7 as

$$I_6 = I_7 = \frac{5\text{x}10^{-12}\cdot 4}{50\text{x}10^{-9}} = 400\mu\text{A}$$

Therefore,

$$\frac{W_6}{L_6} = \frac{2\cdot 400}{(0.5)^2\cdot 50} = 64 \quad \text{and} \qquad \frac{W_7}{L_7} = \frac{2\cdot 400}{(0.5)^2\cdot 110} = 29$$

Next, we guess C_I = 0.2pF. This gives

$$I_5 = \frac{0.2\text{pF}(4\text{V})}{50\text{ns}} = 16\mu\text{A} \quad \rightarrow \qquad I_5 = 20\mu\text{A}$$

Step 5 gives V_{SG3} as 1.2V which results in

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{20}{50(1.2\text{-}0.7)^2} = 1.6 \qquad \rightarrow \qquad \frac{W_3}{L_3} = \frac{W_4}{L_4} = 2$$

Example 8.2-7 - Continued

The desired gain is found to be 4000 which gives an input transconductance of

$$g_{m1} = \frac{4000\cdot 0.09\cdot 10}{44.44} = 81\mu\text{S}$$

This gives the *W*/*L* ratios of M1 and M2 as

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{(81)^2}{110\cdot 40} = 1.49 \quad \rightarrow \qquad \frac{W_1}{L_1} = \frac{W_2}{L_2} = 2$$

To check the guess for C_I we need to calculate it which done as

$$C_I = C_{gd2}+C_{gd4}+C_{gs6}+C_{bd2}+C_{bd4} = 0.9\text{fF}+0.4\text{fF}+119.5\text{fF}+20.4\text{fF}+15.3\text{fF} = 156.5\text{fF}$$

which is less than what was guessed.

Finally, the *W*/*L* value of M5 is found by finding V_{GS1} as 1.00V which gives V_{DS5}(sat) = 0.25V. This gives

$$\frac{W_5}{L_5} = \frac{2\cdot 20}{(0.25)^2\cdot 110} = 5.8 \approx 6$$

As in the previous example, M5 and M7 cannot be connected gate-gate and source-source and a scheme like that of Example 8.2-6 must be used. The *W* values are summarized below assuming that all channel lengths are 1µm.

$W_1 = W_2$ = 2µm $W_3 = W_4$ = 4µm W_5 = 6µm W_6 = 64µm W_7 = 29µm

SECTION 8.3 - OTHER OPEN-LOOP COMPARATORS

Push-Pull Comparators

Clamped:

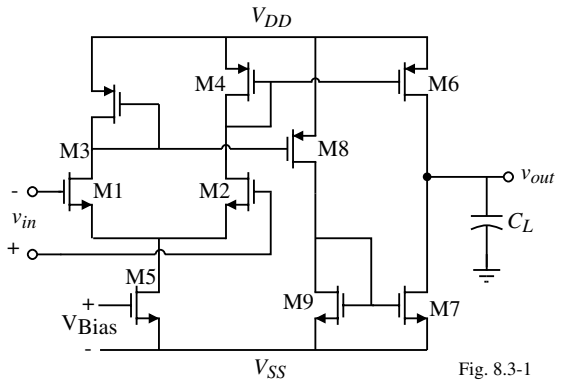


Fig. 8.3-1

Comments:

- Gain reduced → Larger input resolution
- Push-pull output → Higher slew rates

Push-Pull Comparators - Improved

Cascode output stage:

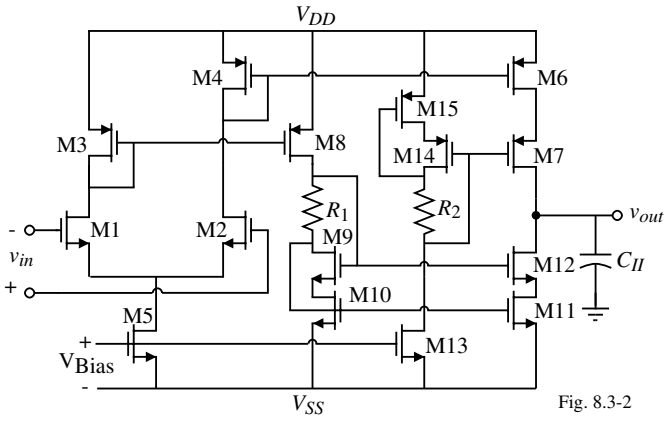


Fig. 8.3-2

Comments:

- Can also use the folded cascode architecture
- Cascode output stage result in a slow linear response (dominant pole is small)
- Poorer noise performance

Comparators that Can Drive Large Capacitive Loads

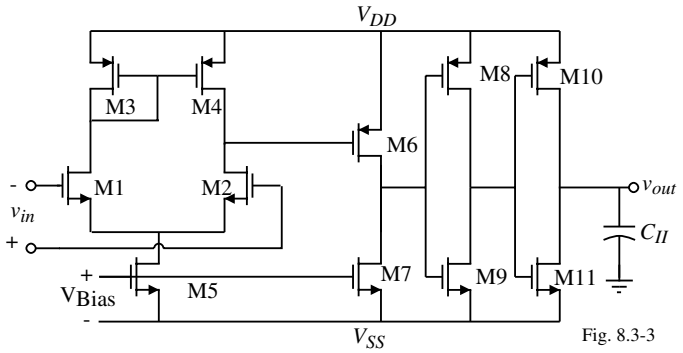


Fig. 8.3-3

Comments:

- Slew rate = 3V/μs into 50pF
- Linear rise/fall time = 100ns into 50pF
- Propagation delay time ≈ 1μs
- Loop gain ≈ 32,000 V/V

Self-Biased Differential Amplifier[†]

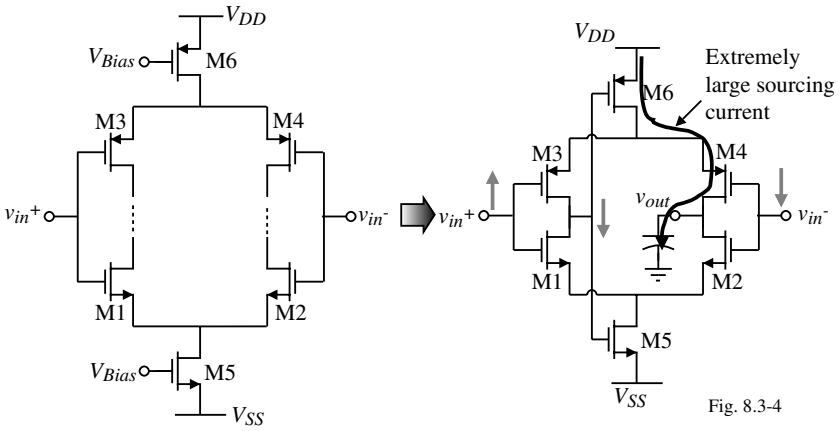


Fig. 8.3-4

Advantage:

Large sink or source current with out a large quiescent current.

Disadvantage:

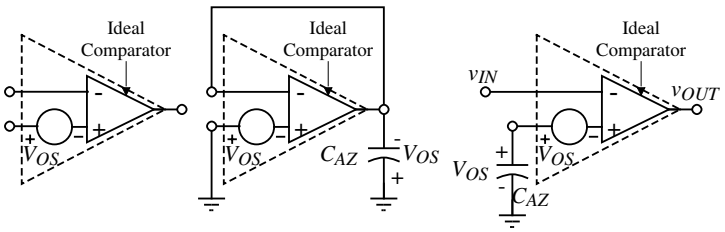
Poor common mode range (v_{in}^+ slower than v_{in}^-)

[†] M. Bazes, "Two Novel Full Complementary Self-Biased CMOS Differential Amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. 26, No. 2, Feb. 1991, pp. 165-168.

SECTION 8.4 IMPROVING THE PERFORMANCE OF THE OPEN-LOOP COMPARATORS

Autozeroing Techniques

Use the comparator as an op amp to sample the dc input offset voltage and cancel the offset during operation.



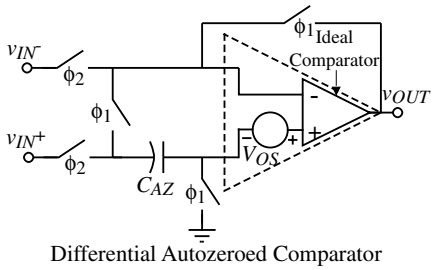
Model of Comparator. Autozero Cycle Comparison Cycle

Fig. 8.4-1

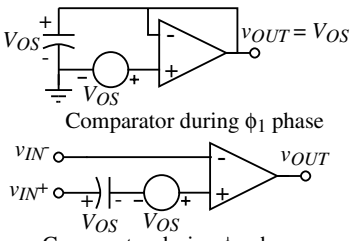
Comments:

- The comparator must be stable in the unity-gain mode (self-compensating comparators are good, the two-stage op comparator would require compensation to be switched in during the autozero cycle.)
- Complete offset cancellation is limited by charge injection

Differential Implementation of Autozeroed Comparators



Differential Autozeroed Comparator



Comparator during ϕ_1 phase

Comparator during ϕ_2 phase

Fig. 8.4-2

Single-Ended Autozeroed Comparators

Noninverting:

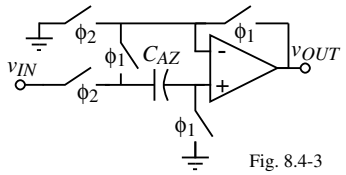


Fig. 8.4-3

Inverting:

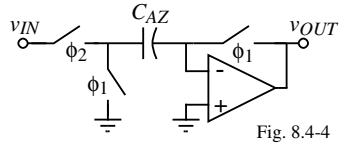


Fig. 8.4-4

Comment on autozeroing:

Need to be careful about noise that gets sampled onto the autozeroing capacitor and is present on the comparison phase of the process.

Influence of Input Noise on the Comparator

Comparator without hysteresis:

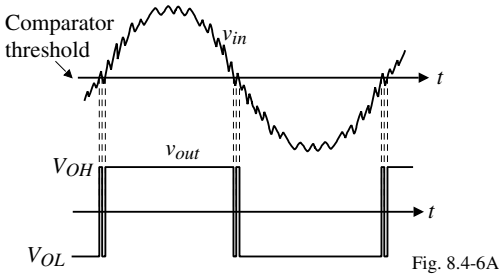


Fig. 8.4-6A

Comparator with hysteresis:

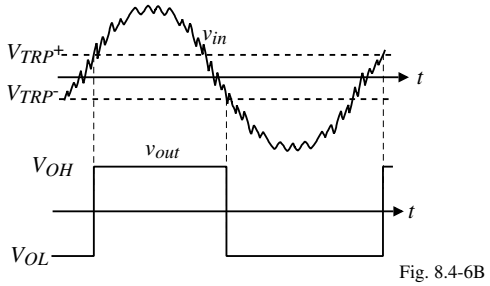
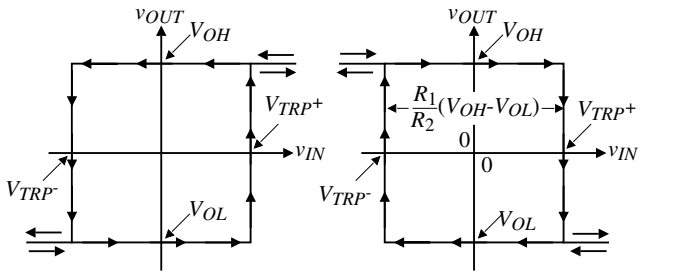


Fig. 8.4-6B

Use of Hysteresis for Comparators in a Noisy Environment

Transfer curve of a comparator with hysteresis:



Counterclockwise Bistable Clockwise Bistable Fig. 8.4-5

Hysteresis is achieved by the use of positive feedback

- Externally
- Internally

Noninverting Comparator using External Positive Feedback

Circuit:

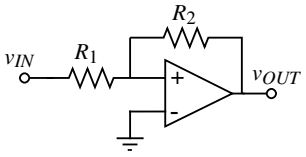
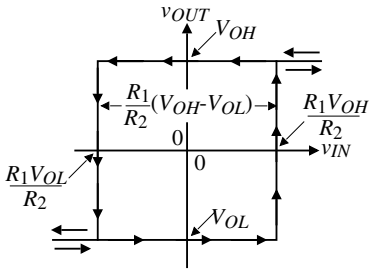


Fig. 8.4-7



Upper Trip Point:

Assume that $v_{OUT} = V_{OL}$, the upper trip point occurs when,

$$0 = \left(\frac{R_1}{R_1+R_2}\right)V_{OL} + \left(\frac{R_2}{R_1+R_2}\right)V_{TRP^+} \qquad \rightarrow \qquad V_{TRP^+} = -\frac{R_1}{R_2}V_{OL}$$

Lower Trip Point:

Assume that $v_{OUT} = V_{OH}$, the lower trip point occurs when,

$$0 = \left(\frac{R_1}{R_1+R_2}\right)V_{OH} + \left(\frac{R_2}{R_1+R_2}\right)V_{TRP^-} \qquad \rightarrow \qquad V_{TRP^-} = -\frac{R_1}{R_2}V_{OH}$$

Width of the bistable characteristic:

$$\Delta V_{in} = V_{TRP^+} - V_{TRP^-} = \left(\frac{R_1}{R_2}\right)(V_{OH} - V_{OL})$$

Inverting Comparator using External Positive Feedback

Circuit:

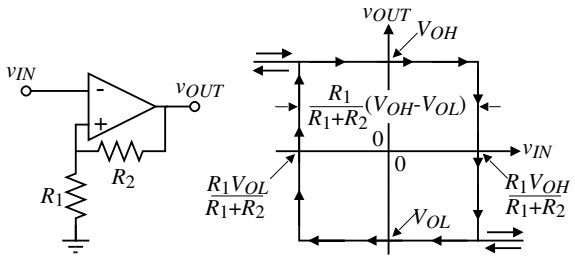


Fig. 8.4-8

Upper Trip Point:

$$v_{IN} = V_{TRP}^{+} = \left(\frac{R_1}{R_1+R_2}\right)V_{OH}$$

Lower Trip Point:

$$v_{IN} = V_{TRP}^{-} = \left(\frac{R_1}{R_1+R_2}\right)V_{OL}$$

Width of the bistable characteristic:

$$\Delta V_{in} = V_{TRP}^{+} - V_{TRP}^{-} = \left(\frac{R_1}{R_1+R_2}\right)(V_{OH} - V_{OL})$$

Horizontal Shifting of the CCW Bistable Characteristic

Circuit:

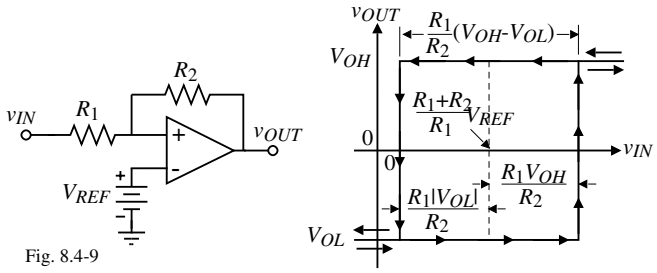


Fig. 8.4-9

Upper Trip Point:

$$V_{REF} = \left(\frac{R_1}{R_1+R_2}\right)V_{OL} + \left(\frac{R_2}{R_1+R_2}\right)V_{TRP}^{+} \quad \rightarrow \quad V_{TRP}^{+} = \left(\frac{R_1+R_2}{R_1}\right)V_{REF} - \frac{R_1}{R_2}V_{OL}$$

Lower Trip Point:

$$V_{REF} = \left(\frac{R_1}{R_1+R_2}\right)V_{OH} + \left(\frac{R_2}{R_1+R_2}\right)V_{TRP}^{-} \quad \rightarrow \quad V_{TRP}^{-} = \left(\frac{R_1+R_2}{R_1}\right)V_{REF} - \frac{R_1}{R_2}V_{OH}$$

Shifting Factor:

$$\left(\frac{R_1+R_2}{R_1}\right)V_{REF}$$

Horizontal Shifting of the CW Bistable Characteristic

Circuit:

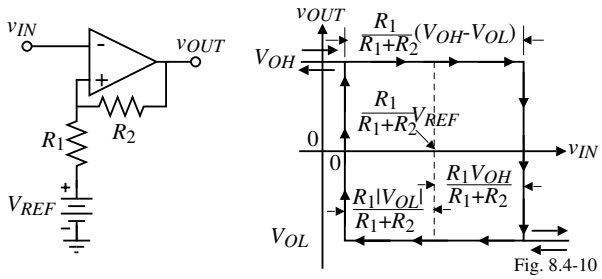


Fig. 8.4-10

Upper Trip Point:

$$v_{IN} = V_{TRP}^{+} = \left(\frac{R_1}{R_1+R_2}\right)V_{OH} + \left(\frac{R_1}{R_1+R_2}\right)V_{REF}$$

Lower Trip Point:

$$v_{IN} = V_{TRP}^{-} = \left(\frac{R_1}{R_1+R_2}\right)V_{OL} + \left(\frac{R_1}{R_1+R_2}\right)V_{REF}$$

Shifting Factor:

$$\left(\frac{R_1}{R_1+R_2}\right)V_{REF}$$

Example 8.4-1 Design of an Inverting Comparator with Hysteresis

Use the inverting bistable to design a high-gain, open-loop comparator having an upper trip point of 1V and a lower trip point of 0V if $V_{OH} = 2$V and $V_{OL} = -2$V.

Solution

Putting the values of this example into the above relationships gives

$$1 = \left(\frac{R_1}{R_1+R_2}\right)2 + \left(\frac{R_1}{R_1+R_2}\right)V_{REF}$$

and

$$0 = \left(\frac{R_1}{R_1+R_2}\right)(-2) + \left(\frac{R_1}{R_1+R_2}\right)V_{REF}$$

Solving these two equations gives $3R_1 = R_2$ and $V_{REF} = 2$V.

Hysteresis using Internal Positive Feedback

Simple comparator with internal positive feedback:

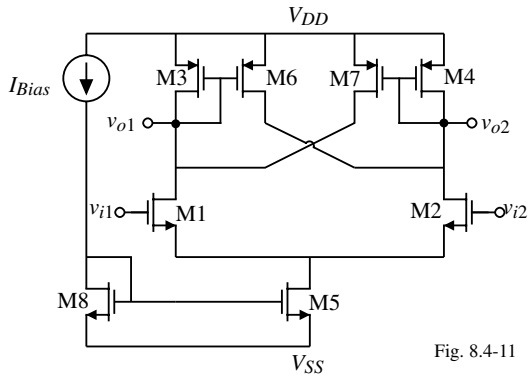


Fig. 8.4-11

Internal Positive Feedback - Upper Trip Point

Assume that the gate of M1 is on ground and the input to M2 is much smaller than zero. The resulting circuit is:

M1 on, M2 off → M3 and M6 on and M4 and M7 off.

∴ v_{o2} is high.

M6 would like to source the current $i_6 = \dfrac{W_6/L_6}{W_3L_3}\, i_1$

As v_{in} begins to increase towards the trip point, the current flow through M2 increases. When $i_2 = i_6$, the upper trip point will occur.

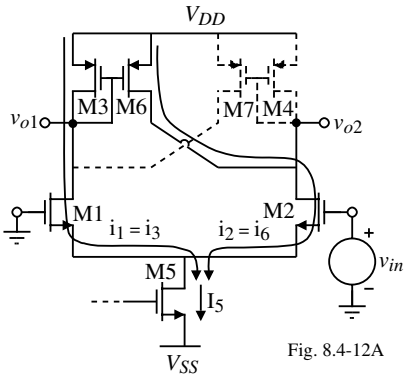


Fig. 8.4-12A

$$\therefore \quad i_5 = i_1+i_2 = i_3+i_6 = i_3 + \left(\frac{W_6/L_6}{W_3/L_3}\right) i_3 = i_3\left[1 + \frac{W_6/L_6}{W_3/L_3}\right]$$

which gives

$$i_1 = i_3 = \frac{i_5}{1 + [(W_6/L_6)/(W_3/L_3)]}$$

Also, $i_2 = i_5 - i_1 = i_5 - i_3$

Knowing i_1 and i_2 allows the calculation of v_{GS1} and v_{GS2} which gives

$$V_{TRP}^{+} = v_{GS2} - v_{GS1} = \sqrt{\frac{2i_2}{\beta_2}} + V_{T2} - \sqrt{\frac{2i_1}{\beta_1}} - V_{T1}$$

Internal Positive Feedback - Lower Trip Point

Assume that the gate of M1 is on ground and the input to M2 is much greater than zero. The resulting circuit is:

M2 on, M1 off → M4 and M7 on and M3 and M6 off.

∴ v_{o1} is high.

M7 would like to source the current $i_7 = \frac{W_7/L_7}{W_4/L_4} i_2$

As v_{in} begins to decrease towards the trip point, the current flow through M1 increases. When $i_1 = i_7$, the lower trip point will occur.

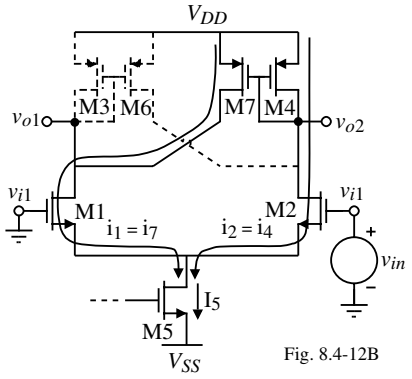


Fig. 8.4-12B

$$\therefore \quad i_5 = i_1+i_2 = i_7+i_4 = \left(\frac{W_7/L_7}{W_4/L_4}\right) i_4 + i_4 = i_4\left[1 + \frac{W_7/L_7}{W_4/L_4}\right] \quad \text{which gives}$$

$$i_2 = i_4 = \frac{i_5}{1 + [(W_7/L_7)/(W_4/L_4)]}$$

Also, $i_1 = i_5 - i_2 = i_5 - i_4$

Knowing i_1 and i_2 allows the calculation of v_{GS1} and v_{GS2} which gives

$$V_{TRP}^- = v_{GS2} - v_{GS1} = \sqrt{\frac{2i_2}{\beta_2}} + V_{T2} - \sqrt{\frac{2i_1}{\beta_1}} - V_{T1}$$

Example 8.4-2 - Calculation of Trip Voltages for a Comparator with Hysteresis

Consider the circuit shown. Using the transistor device parameters given in Table 3.1-2 calculate the positive and negative threshold points if the device lengths are all 1 m and the widths are given as: $W_1 = W_2 = W_6 = W_7 = 10$ m and $W_3 = W_4 = 2$ m. The gate of M1 is tied to ground and the input is the gate of M2. The current, $i_5 = 20$ A. Simulate the results using PSPICE.

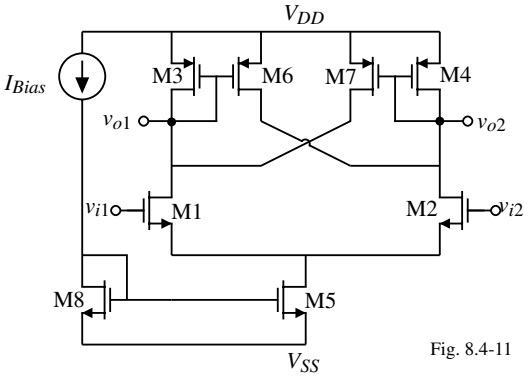


Fig. 8.4-11

Solution

To calculate the positive trip point, assume that the input has been negative and is heading positive.

$$i_6 = \frac{(W/L)_6}{(W/L)_3} i_3 = (5/1)(i_3)$$

$$i_3 = \frac{i_5}{1 + [(W/L)_6/(W/L)_3]} = i_1 = \frac{20 \text{ A}}{1 + 5} = 3.33 \text{ A}$$

$$i_2 = i_5 - i_1 = 20 - 3.33 = 16.67 \text{ A}$$

$$v_{GS1} = \left(\frac{2i_1}{\beta_1}\right)^{1/2} + V_{T1} = \left(\frac{2 \cdot 3.33}{(5)110}\right)^{1/2} + 0.7 = 0.81\text{V}$$

$$v_{GS2} = \left(\frac{2i_2}{\beta_2}\right)^{1/2} + V_{T2} = \left(\frac{2 \cdot 16.67}{(5)110}\right)^{1/2} + 0.7 = 0.946\text{V}$$

$$V_{TRP+} \cong v_{GS2} - v_{GS1} = 0.946 - 0.810 = 0.136\text{V}$$

Example 8.4-2 - Continued

Determining the negative trip point, similar analysis yields

$i_4 = 3.33$ A
$i_1 = 16.67$ A
$v_{GS2} = 0.81$V
$v_{GS1} = 0.946$V
$V_{TRP-} \cong v_{GS2} - v_{GS1} = 0.81 - 0.946 = -0.136$V

PSPICE simulation results of this circuit are shown below.

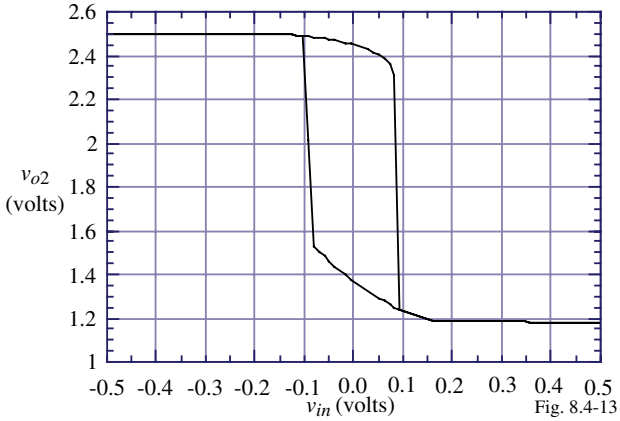


Fig. 8.4-13

Complete Comparator with Internal Hysteresis

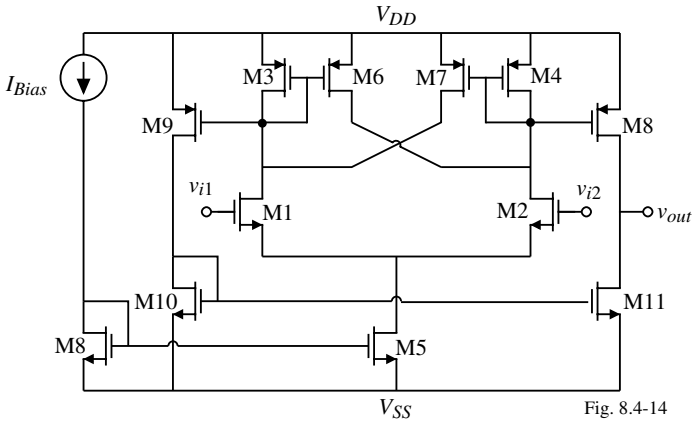


Fig. 8.4-14

Schmitt Trigger

The Schmitt trigger is a circuit that has better defined switching points.

Consider the following circuit:

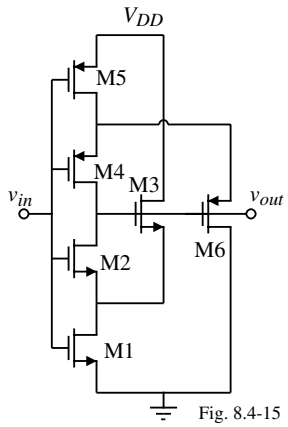


Fig. 8.4-15

How does this circuit work?

Assume the input voltage, v_{in}, is low and the output voltage, v_{out} , is high.

$\therefore$ M3, M4 and M5 are on and M1, M2 and M6 are off.

When v_{in} is increased from zero, M2 starts to turn on causing M3 to start turning off. Positive feedback causes M2 to turn on further and eventually both M1 and M2 are on and the output is at zero.

The upper switching point, V_{TRP}^+ is found as follows:

When v_{in} is low, the voltage at the source of M2 (M3) is

$$v_{S2} = V_{DD}-V_{TN3}$$

V_{TRP}^+ is defined as the point when M2 turns on given as

$$V_{TRP}^+ = V_{TN2} + v_{S2}$$

V_{TRP}^+ occurs at the point where the input voltage causes the current in M3 to equal the current in M1.

Thus, $i_{D1} = \beta_1(V_{TRP}^+ - V_{TN1})^2 = \beta_3(V_{DD} - v_{S2} - V_{TN3})^2 = i_{D3}$

which can be written as, assuming that $V_{TN2} = V_{TN3}$,

$$\beta_1(V_{TRP}^+ - V_{TN1})^2 = \beta_3(V_{DD} - V_{TRP}^+)^2 \quad \Rightarrow \quad V_{TRP}^+ = \frac{V_{TN1} + \sqrt{\frac{\beta_3}{\beta_1}}\,V_{DD}}{1 + \sqrt{\frac{\beta_3}{\beta_1}}}$$

Schmitt Trigger – Continued

The switching point, V_{TRP}^- is found in a similar manner and is:

$$\beta_5(V_{DD} - V_{TRP}^- - V_{TP5})^2 = \beta_6(V_{TRP}^-)^2 \quad \Rightarrow \quad V_{TRP}^- = \frac{\sqrt{\frac{\beta_5}{\beta_6}}(V_{DD} - V_{TP5})}{1 + \sqrt{\frac{\beta_5}{\beta_6}}}$$

The bistable characteristic is,

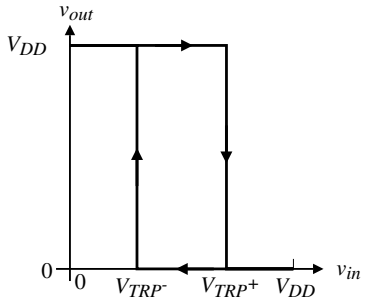
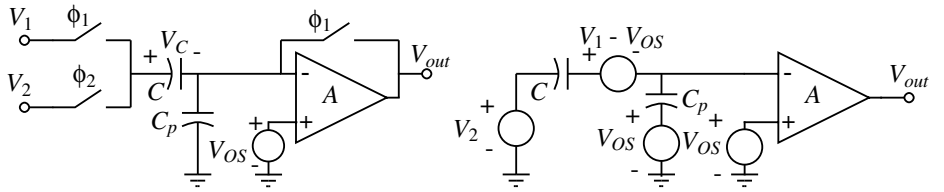


Fig. 8.4-16

SECTION 8.5 - DISCRETE-TIME COMPARATORS

Switched Capacitor Comparator



A switched capacitor comparator Equivalent circuit when the ϕ_2 switches are closed

Fig. 8.5-1

ϕ_1 Phase:

The V_1 input is sampled and the dc input offset voltage is autozeroed.

$$V_C(\phi_1) = V_1 - V_{OS} \qquad \text{and} \qquad V_{Cp}(\phi_1) = V_{OS}$$

ϕ_2 Phase:

$$V_{out}(\phi_2) = -A\left[\frac{V_2 C}{C+C_p} - \frac{(V_1-V_{OS})C}{C+C_p} + \frac{V_{OS}C_p}{C+C_p}\right] + AV_{OS}$$

$$= -A\left[(V_2-V_1)\frac{C}{C+C_p} + V_{OS}\left(\frac{C}{C+C_p} + \frac{C_p}{C+C_p}\right)\right] + AV_{OS} = -A(V_2-V_1)\frac{C}{C+C_p} \approx A(V_1-V_2)$$

if C_p is smaller than C.

Differential-In, Differential-Out Switched Capacitor Comparator

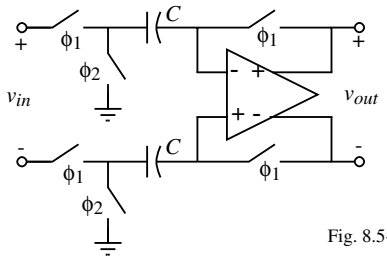


Fig. 8.5-2

Comments:

- Reduces the influence of charge injection
- Eliminates even harmonics

Regenerative Comparators

Regenerative comparators use positive feedback to accomplish the comparison of two signals. Latches have a faster switching speed that the previous bistable comparators.

NMOS and PMOS latch:

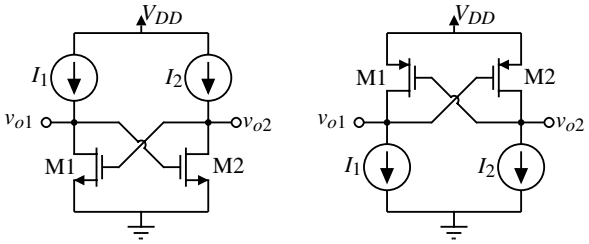


Fig. 8.5-3

How is the input applied to a latch?

The inputs are initially applied to the outputs of the latch.

V_{o1}' = initial input applied to v_{o1}

V_{o2}' = initial input applied to v_{o2}

Step Response of a Latch

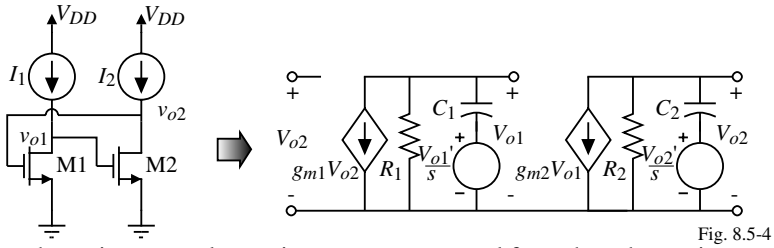


Fig. 8.5-4

where R_i and C_i are the resistance and capacitance seen to ground from the i-th transistor.

Nodal equations:

$$g_{m1}V_{o2}+G_1V_{o1}+sC_1\left(V_{o1}-\frac{V_{o1}'}{s}\right)=g_{m1}V_{o2}+G_1V_{o1}+sC_1V_{o1}-C_1V_{o1}'=0$$

$$g_{m2}V_{o1}+G_2V_{o2}+sC_2\left(V_{o2}-\frac{V_{o2}'}{s}\right)=g_{m2}V_{o1}+G_2V_{o2}+sC_2V_{o2}-C_2V_{o2}'=0$$

Solving for V_{o1} and V_{o2} gives,

$$V_{o1}=\frac{R_1C_1}{sR_1C_1+1}V_{o1}'-\frac{g_{m1}R_1}{sR_1C_1+1}V_{o2}=\frac{\tau_1}{s\tau_1+1}V_{o1}'-\frac{g_{m1}R_1}{s\tau_1+1}V_{o2}$$

$$V_{o2}=\frac{R_2C_2}{sR_2C_2+1}V_{o2}'-\frac{g_{m2}R_2}{sR_2C_2+1}V_{o1}=\frac{\tau_2}{s\tau_2+1}V_{o2}'-\frac{g_{m2}R_2}{s\tau_2+1}V_{o1}$$

Defining the output, ΔV_o, and input, ΔV_i, as

$$\Delta V_o=V_{o2}-V_{o1} \qquad \text{and} \qquad \Delta V_i=V_{o2}'-V_{o1}'$$

Step Response of the Latch - Continued

Solving for ΔV_o gives,

$$\Delta V_o = V_{o2}\text{-}V_{o1} = \frac{\tau}{s\tau+1}\Delta V_i + \frac{g_m R}{s\tau+1}\Delta V_o$$

or

$$\Delta V_o = \frac{\tau\,\Delta V_i}{s\tau+(1\text{-}g_m R)} = \frac{\frac{\tau\,\Delta V_i}{1\text{-}g_m R}}{\frac{s\tau}{1\text{-}g_m R}+1} = \frac{\tau'\,\Delta V_i}{s\tau'+1}$$

where

$$\tau' = \frac{\tau}{1\text{-}g_m R}$$

Taking the inverse Laplace transform gives

$$\Delta v_o(t) = \Delta V_i'\, e^{-t/\tau} = \Delta V_i\, e^{-t(1-g_m R)/\tau} \approx e^{g_m R t/\tau}\Delta V_i, \quad \text{if } g_m R >> 1.$$

Define the latch time constant as

$$\tau_L \approx \frac{\tau}{g_m R} = \frac{C}{g_m} = \frac{0.67WLC_{ox}}{\sqrt{2K'(W/L)I}} = 0.67C_{ox}\sqrt{\frac{WL^3}{2K'I}}$$

if $C \approx C_{gs}$.

$\therefore \quad \Delta V_{out}(t) = e^{t/\tau_L}\,\Delta V_i$

Step Response of a Latch - Continued

Normalize the output voltage by $(V_{OH}\text{-}V_{OL})$ to get

$$\frac{\Delta V_{out}(t)}{V_{OH}\text{-}V_{OL}} = e^{t/\tau_L}\frac{\Delta V_i}{V_{OH}\text{-}V_{OL}}$$

which is plotted as,

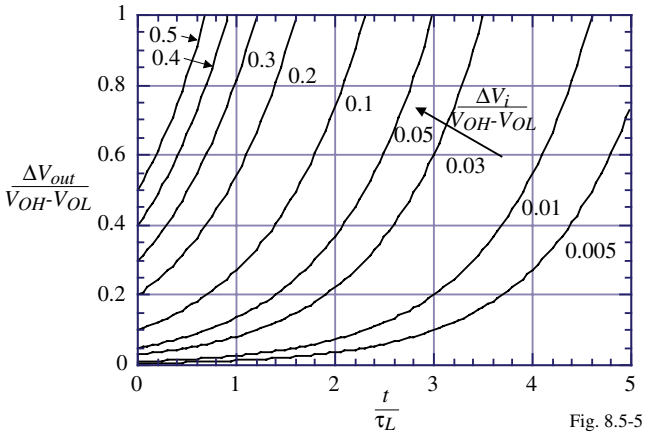


Fig. 8.5-5

The propagation delay time is $t_p = \tau_L\, ln\left(\frac{V_{OH}\text{-}\,V_{OL}}{2\Delta V_i}\right)$

Example 8.5-1 - Time domain characteristics of a latch.

Find the time it takes from the time the latch is enabled until the output voltage, ΔV_{out}, equals V_{OH}-V_{OL} if the W/L of the latch NMOS transistors is 10μm/1μm and the latch dc current is 10μA when ΔV_i = $0.1(V_{OH}$-$V_{OL})$ and ΔV_i = $0.01(V_{OH}$-$V_{OL})$. Find the propagation time delay for the latch for each of these conditions.

Solution

The transconductance of the latch transistors is

$$g_m = \sqrt{2 \cdot 110 \cdot 10 \cdot 10} = 148\mu S$$

The output conductance is 0.4μS which gives $g_m R$ of 59.2V/V. Since $g_m R$ is greater than 1, we can use the above results. Therefore the latch time constant is found as

$$\tau_L = 0.67 C_{ox} \sqrt{\frac{WL^3}{2K'I}} = 0.67(24\text{x}10^{-4}) \sqrt{\frac{(10 \cdot 1)\text{x}10^{-18}}{2 \cdot 110\text{x}10^{-6} \cdot 10\text{x}10^{-6}}} = 108\text{ns}$$

If we assume that the propagation time delay is the time when the output is $0.5(V_{OH}$-$V_{OL})$, then using the above results or Fig. 8.5-5 we find for $\Delta V_i = 0.01(V_{OH}$-$V_{OL})$ that $t_p = 3.91\tau_L$ = 422ns and for ΔV_i = $0.1(V_{OH}$-$V_{OL})$ that $t_p = 2.3\tau_L$ = 174ns.

If we assume that the propagation time delay is the time for the output to reach $(V_{OH}$-$V_{OL})$, then for ΔV_i = $0.01(V_{OH}$-$V_{OL})$ that $t_p = 4.602\tau_L$ = 497ns and for $\Delta V_i = 0.1(V_{OH}$-$V_{OL})$ that $t_p = 2.306\tau_L$ = 249ns.

Comparator using a Latch with a Built-In Threshold[†]

How does it operate?

1.) Devices in shaded region operate in the triode region.

2.) When the latch/reset goes high, the upper cross-coupled inverter-latch regenerates. The drain currents of M5 and M6 are steered to obtain a final state determined by the mismatch between the R_1 and R_2 resistances.

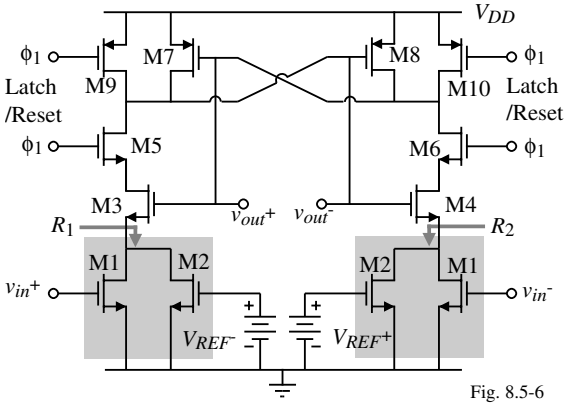


Fig. 8.5-6

$$\frac{1}{R_1} = K_N \left[\frac{W_1}{L}(v_{in}^+ - V_T) + \frac{W_2}{L}(V_{REF}^- - V_T) \right]$$

and

$$\frac{1}{R_2} = K_N \left[\frac{W_1}{L}(v_{in}^- - V_T) + \frac{W_2}{L}(V_{REF}^+ - V_T) \right]$$

3.) The input voltage which causes R_1 and R_2 to be equal is given by

$v_{in}(\text{threshold}) = (W_2/W_1)V_{REF}$

W_2/W_1 = 1/4 generates a threshold of $\pm 0.25 V_{REF}$.

Performance → 20Ms/s & 200μW

[†] T.B. Cho and P.R. Gray, "A 10b, 20Msamples/s, 35mW pipeline A/D Converter," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 166-172, March 1995.

Simple, Low Power Latched Comparator[†]

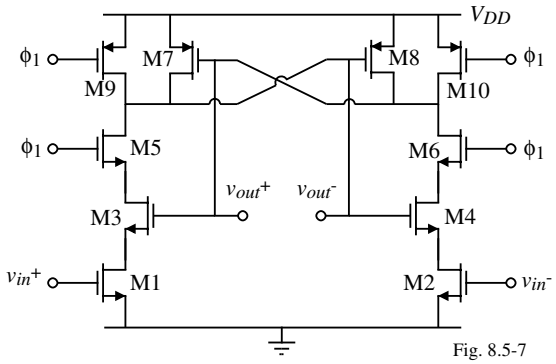


Fig. 8.5-7

Dissipated 50μW when clocked at 2MHz.

[†] A. Coban, "1.5V, 1mW, 98-dB Delta-Sigma ADC", Ph.D. dissertation, School of ECE, Georgia Tech, Atlanta, GA 30332-0250.

Dynamic Latch

Circuit:

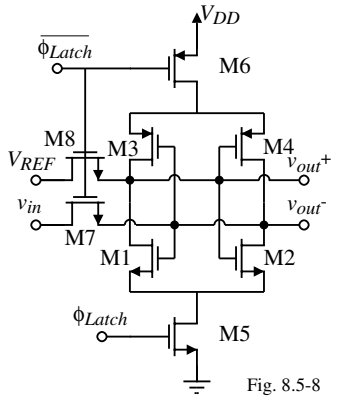


Fig. 8.5-8

Input offset voltage distribution:

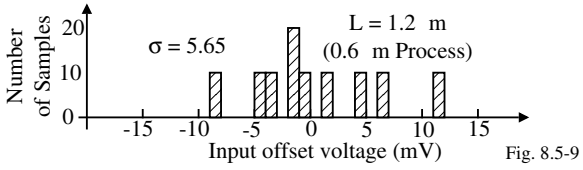


Fig. 8.5-9

Power dissipation/sampling rate = 4.3μW/Ms/s

SECTION 8.6 - HIGH-SPEED COMPARATORS

Conceptual Illustration of a Cascaded Comparator

How does a cascaded, high-speed comparator work?

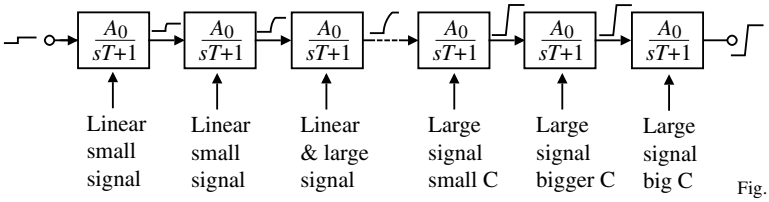


Fig. 8.6-1

Assuming a small overdrive,

1.) The initial stage build the driving capability.

2.) The latter stages swing rail-to-rail and build the ability to quickly charge and discharge capacitance.

Minimizing the Propagation Delay Time in Comparators

Fact:

- The input signal is equal to V_{in}(min) for worst case
- Amplifiers have a step response with a negative argument in the exponential
- Latches have a step response with a positive argument in the exponential

Result:

Use a cascade of linear amplifier to quickly build up the signal level and apply this amplified signal level to a latch for quick transition to the full binary output swing.

Illustration of a preamplifier and latch cascade:

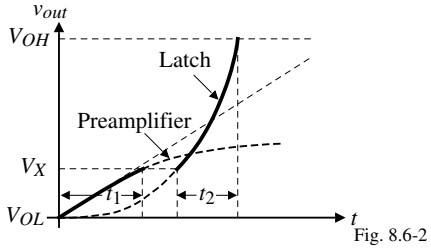


Fig. 8.6-2

Minimization of t_p:

Q. If the preamplifer consists of n stages of gain A having a single-pole response, what is the value of n and A that gives minimum propagation delay time?

A. $n = 6$ and $A = 2.62$ but this is a very broad minimum and n is usually 3 and $A \approx$ 6-7 to save area.

Fully Differential, Three-Stage Amplifier and Latch Comparator

Circuit:

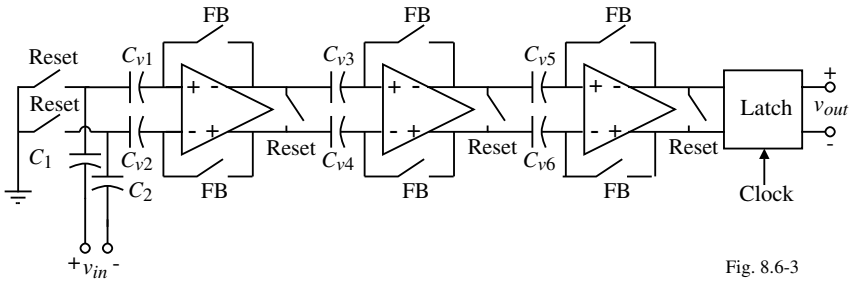


Fig. 8.6-3

Comments:

- Autozero and reset phase followed by comparison phase
- More switches are needed to accomplish the reset and autozero of all preamplifiers simultaneously
- Can run as high as 100Msps

Preamplifier and Latch Circuits

Gain:

$$A_v = -\frac{g_{m1}}{g_{m3}} = -\frac{g_{m2}}{g_{m4}} = -\sqrt{\frac{K_N'(W_1/L_1)}{K_p'(W_3/L_3)}}$$

Dominant Pole:

$$|p_{dominant}| = \frac{g_{m3}}{C} = \frac{g_{m4}}{C}$$

where C is the capacitance seen from the output nodes to ground.

If $(W_1/L_1)/(W_3/L_3) = 100$ and the bias current is 100μA, then $A = -3.85$ and the bandwidth is 15.9MHz if $C = 0.5$pF.

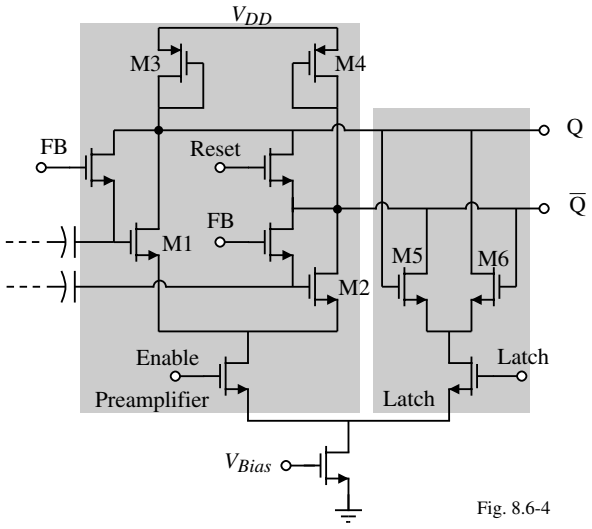


Fig. 8.6-4

Comments:

- If a buffer is used to reduce the output capacitance, one must take into account the loss of the buffer.
- The use of a preamplifier before the latch reduces the latch offset by the gain of the preamplifier so that the offset is due to the preamplifier only.

An Improved Preamplifier

Circuit:

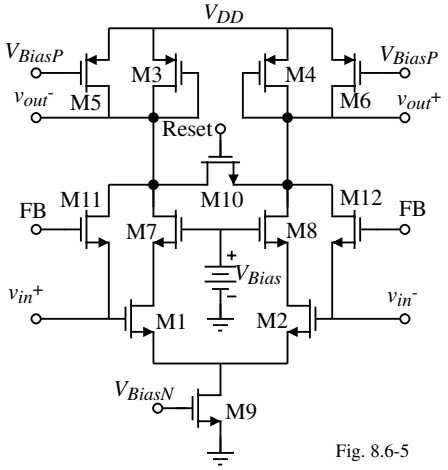


Fig. 8.6-5

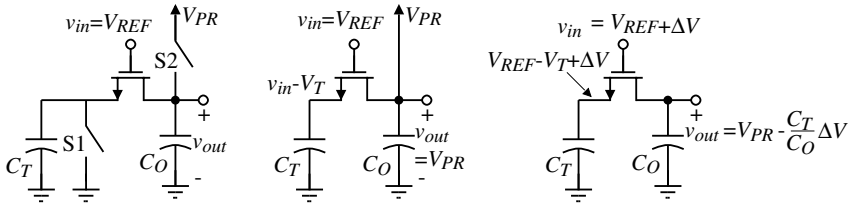
Gain:

$$A_v = -\frac{g_{m1}}{g_{m3}} = -\sqrt{\frac{K_N'(W_1/L_1)I_1}{K_P'(W_3/L_3)I_3}} = -\sqrt{\frac{K_N'(W_1/L_1)}{K_P'(W_3/L_3)}}\sqrt{1+\frac{I_5}{I_3}}$$

If $I_5 = 24I_3$, the gain is increased by a factor of 5

Charge Transfer Preamplifier

The preamplifier can be replaced by the charge transfer circuit shown.



Charge transfer amplifier. Precharge phase. Amplification phase.

Fig. 8.6-6

Comments:

- Only positive values of voltage will be amplified.
- Large offset voltages result as a function of the subthreshold current.

A CMOS Charge Transfer Preamplifier

Circuit:

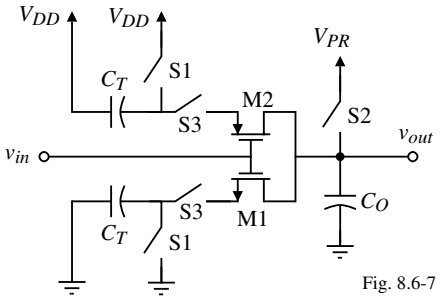


Fig. 8.6-7

Comments:

- NMOS and PMOS allow both polarities of input
- CMOS switches along with dummy switches reduce the charge injection
- Switch S3 prevents the subthreshold current influence
- Used as a preamplifier in a comparator with 8-bit resolution at 20Msps and a power dissipation of less than 5μW

A High-Speed Comparator

Circuit:

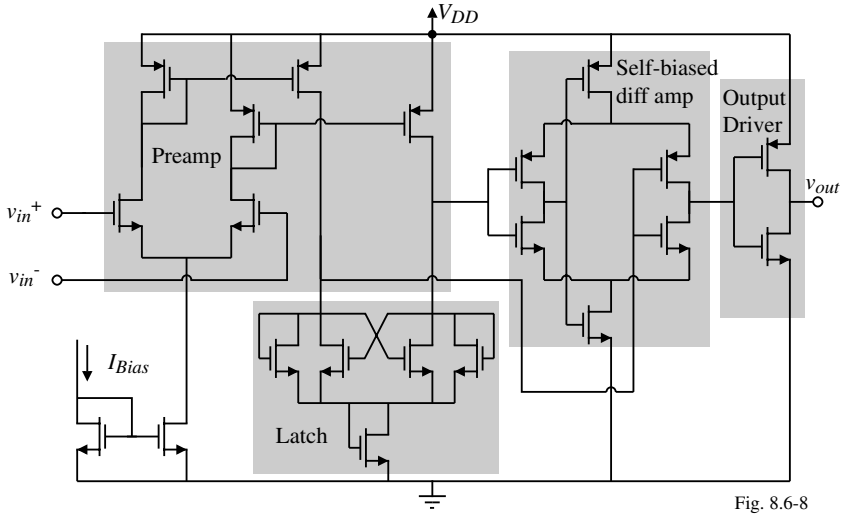


Fig. 8.6-8

Comments:

- Designed to have a t_p = 10ns with a 5pF load and a 10mV overdrive
- Not synchronous
- Comparator gain is greater than 2000V/V and the quiescent current was 100μA

SECTION 8.7 - SUMMARY

Types of Comparators Presented

- High-gain, open-loop
- Improved high-gain, open-loop, comparators
  - Hysteresis
  - Autozeroing
- Regenerative comparators
- Discrete-time comparators

Performance Characterization

- Propagation delay time
- Binary output swing
- Input resolution and/or gain
- Input offset voltage
- Power dissipation

Important Principles

- The speed of the comparator depends on the linear and slewing responses
- The dc input offset voltage depends on the matching and can be reduced by autozeroing.
  - Charge injection is the limit of autozeroing
- The gain of the comparator should be large enough for a binary output when $v_{in} = V_{in}(\min)$
- In cascaded comparators, the early stages should have wide bandwidth and the latter stages high slew rate

